Digital To Analog Converter (DAC)

Digital to analog converter is used to convert digital quantity into analog quantity. DAC converter produces an output current of voltage proportional to digital quantity (binary word) applied to its input. Today microcomputers are widely used for industrial control. The output of the microcomputer is a digital quantity. In many applications the digital output of the microcomputer has to be converted into analog quantity which is used for the control of relay, small motor, actuator e.t.c. In communication system digital transmission is faster and convenient but the digital signals have to be converted back to analog signals at the receiving terminal. DAC converters are also used as a part of the circuitry of several ADC converters.

There are several ways of making a digital to analog converter. Some of them are given as under.

1. Binary weighted resistor DAC
2. R-2R Ladder network
3. Serial DAC converter
4. BCD DAC
5. Bipolar DAC

Binary weighted Resistor DAC

A binary weighted resistor ladder D/A converter is shown in figure 1.

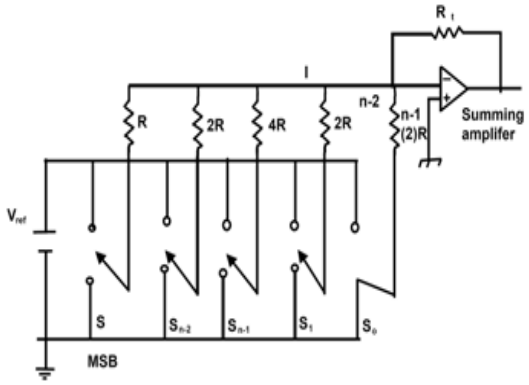


Figure 1: A Binary weighted D/A Converter

Figure 1: Binary Weighted DAC

It consists of the following four major components.

1. n switches one for each bit applied to the input
2. a weighted resistor ladder network, where the resistance are inversely proportional to the numerical significance of the corresponding binary digital
3. a reference voltage V_{ref} and
4. a summing amplifier that adds the current flowing in the resistive network to develop a signal that is proportional to the digital input.

The behavior of the circuit may be analyzed easily by using "**Millman's theorem**". It state that "***the voltage appearing at any node in a resistive network is equal to the summation of the current entering the node (assuming the node voltage is zero) divided by the summation of the conductance connected to the mode***".

Mathematically we can write

$$V_o = \frac{\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R} + \cdots \frac{V_n}{(2^{n-1})R}}{\left[\frac{1}{R} + \frac{1}{2R} + \frac{1}{4R} + \cdots \frac{1}{(2^{n-1})R}\right]}$$

Assume that the resistor R_1, R_2, R_3 ..... R_n are binary weighted resistors, thus

$R_1 = R$

$R_2 = 2R$

$R_3 = 4R$

.....

.....

.....

$R_n = (2^{n-1}) R$

$$V_o = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right]}$$

A Resistor Ladder Network, can delivers a binary number say number of n bits.

$$N = a_{n-1} z^{n-1} + a_{n-2} z^{n-2} + \cdots a_1 2^1 + a_0 2^0$$

Or

$$= \sum_{i=0}^{n-1} a_i \, . z^i \, , where \; a_i = \{0,1\}$$

Each bit controls a switch s_i that is connected to V_{ref}.

when $a_i = 1$, then bit is ON, and when $a_i = 0$, then bit is OFF.

The reference voltage source V_R is considered to have zero internal impedance. The resistor that are connected to the switches have value such as to make the current flow proportion to the binary weight of the respective input. But the resistor in the MSB position has the value R, the next has the value 2R etc. The resistor of the LSB have the value of (2^{n-1}) R.

The current flowing in the summing amplifier is

$$I = \frac{a_{n-1} V_R}{R} + \frac{a_{n-2} V_R}{2R} + \cdots \; \frac{a_1 V_R}{(2)^{n-1} R}$$

Multiplying and dividing by $(2)^{n-1}$ R

$$I = \frac{V_R}{(2)^{n-1} R} [a_{n-1} 2^{n-1} + a_{n-2} 2^{n-1} . 2^{-1} + \cdots + a_n 2^{n-1} . 2^{-n+2} + a_o (2^o)]$$

$$I = \frac{V_R}{(2)^{n-1} R} [a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \cdots + a_1 2^1 + a_o 2^o] 2^o = 1$$

or

$$I = \frac{V_R}{(2)^{n-1} R} \sum_{i=0}^{n-1} a_i z^i$$

$$I_{max} = \frac{V_R}{(2)^{n-1}R}(2^n - 1)$$

When all the bits of digital word have value of 1, then the output current of D/A converter is termed the full scale output current and is an important design parameter.

On the other hand, if all switches are open i.e. all a_i coefficients are zero, then the output voltage (current) is zero.

The maximum output voltage $V_o = -R_f I$ depends on the feedback resistor R_f. As, the operational amplifier is operated in the negative feedback mode for the purpose of summing so that it performs as an excellent current to voltage converter.

Advantages

As only one resistor is used per it in the resistor network, thus it is an economical D/A converter.

Disadvantages / Limitations

1. Resistors used in the network have a wide range of values, so it is very difficult to ensure the absolute accuracy and stability of all the resistors.
2. It is very difficult to match the temperature coefficients of all the resistors. This factor is specially important in D/A converters operation over a wide temperature range.
3. When n is so large, the resistance corresponding to LBS can assume a large value, which may be comparable with the input resistance of the amplifier. This leads to erroneous results.
4. As the switches represent finite impedance that are connected in series with the weighted resistors and their magnitudes and variations have to be taken in to account in a D/A converter design.

R-2R Ladder Network

In case of weighted resistor DAC requires a wide range of resistance values and switches for each bit position if high accuracy conversion is required. A digital to analog converter with an R-2R ladder network as shown in figure 2

eliminates these complications at the expense of an additional resistor for each bit.

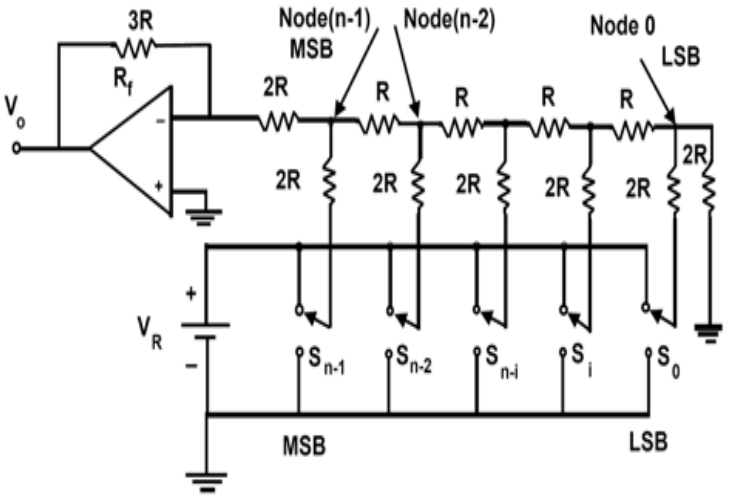


Figure 2: DAC Employing R-2R Ladder Network

Figure 2: DAC Employing R-2R Ladder Network

The operation of R-2R ladder DAC is easily explained considering the weights of the different bits one at a time. This can be followed by superposition to construct analog output corresponding any digital input word. Let only the MSB is turned ON in the first case, and all other bits are OFF, a simplified equivalent circuit can be drawn as shown in figure 3.

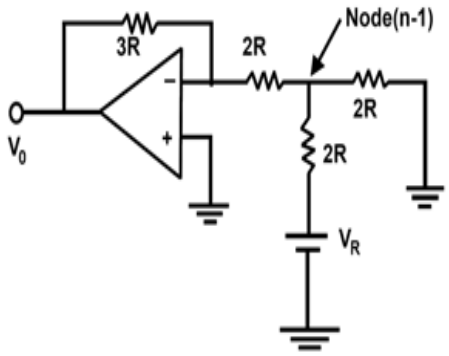


Figure 3: Equivalent Circuit for R-2R ladder network,
when MSB is ON and all other are OFF

The equivalent circuit with only switch S_{n-2} connected to the reference voltage is shown in figure 4.

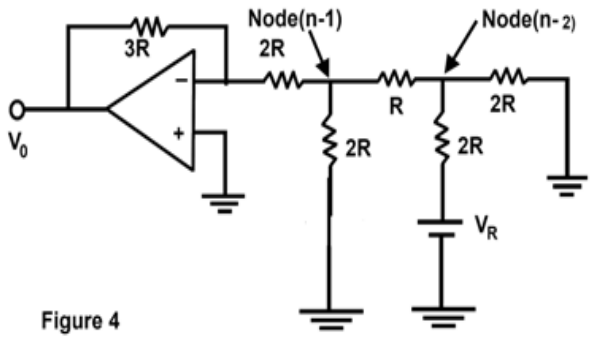


Figure 4

By using principle of superposition all contributions are summed up and the resultant output is

$V_0 = V_R [a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + ...a_1 2^{-(n-1)} + a_0 2^{-n}]$

$V_0 = V_R 2^{-n} [a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + ...a_1 2^{+1} + a_0 2^{0}]$

$$= -V_R 2^{-n} \sum_{i=0}^{n-1} a_i 2^i ; where\ a_i \in \{0,1\}$$

Note that a_i depends on whether th *i*the switch is at 0 or at V_R. Thus the output of the DAC is proportional to the sum of the weights represented by thosee switches that are connected to V_R and the ratio of resistors in the R-2R ladder network.

From this circuit, voltage at mode (n-1) is given by

$V_{n-1} = V_R (R/3R)(-3R) = V_R/3$

As the input terminal of the operational amplifier is at virtual ground. If the feedback resistor R_f for the operational amplifier is taken as 3R, the corresponding output voltage du to the MSB alone is

$V_0 = (V_R / 3) (-3R / 2R)$

$= - V_R / 2$

Let next switch S_{n-2} at V_R with all other switches at zero. Here, the current at node (n - 2) divide equally to the right and to the left resulting in a voltage at node (n - 2)

$V_{n-2} = V_R / 3$

This voltage is attenuated by a factor of 2 at node (n - 1), as

$V_{n-1} = V_{n-2} (R / 2R) = V_R / 6$

Output voltage due to node n-2 at the operational amplifier is

$V_0 = (V_R / 6) (-3R / 2R)$

$= - V_R / 4$

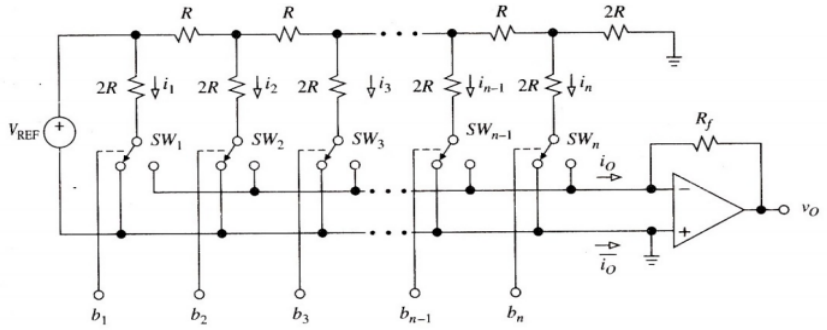
Advantages

1. Only two values of resistors are used; R and 2R.
2. The actual value used for R is relatively less important as long as extremely large values, where stray capacitance enter the picture, are not employs only ratio of resistor values is critical.
3. R-2R ladder network are available in monolithic chips,. These are laser trimmed to be within 0.01% of the desired ratios.
4. The staircase voltage is more likely to be monotonic as the effect of the MSB resistor is not many times grater than that for LSB resistor.

INVERTED OR CURRENT AND VOLTAGE MODE DAC

INVERTED OR CURRENT MODE DAC

As the name implies, Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into i1 , i2, i3 .....in. in each arm. The currents are either diverted to the ground bus (io) or to the Virtual-ground bus ($\overline{io}$).



The currents are given as

i1 = VREF/2R = (VREF/R) 2-1, i2 = (VREF)/2)/2R = (VREF/R) 2-2.....in = (VREF/R) 2-n.

And the relationship between the currents are given as

i2 = i1/2

i3 = i1/4

i4 = i1/8

in = i1/2n-1

Using the bits to identify the status of the switches, and letting V0 = -Rf io gives

V0 = - (Rf/R) VREF (b12-1 + b22-2+ ……. + bn2-n)

The two currents io and $\overline{io}$ are complementary to each other and the potential of io bus must be sufficiently close to that of the $\overline{io}$ bus. Otherwise, linearity errors will occur. The final op-amp is used as current to voltage converter.

Advantages

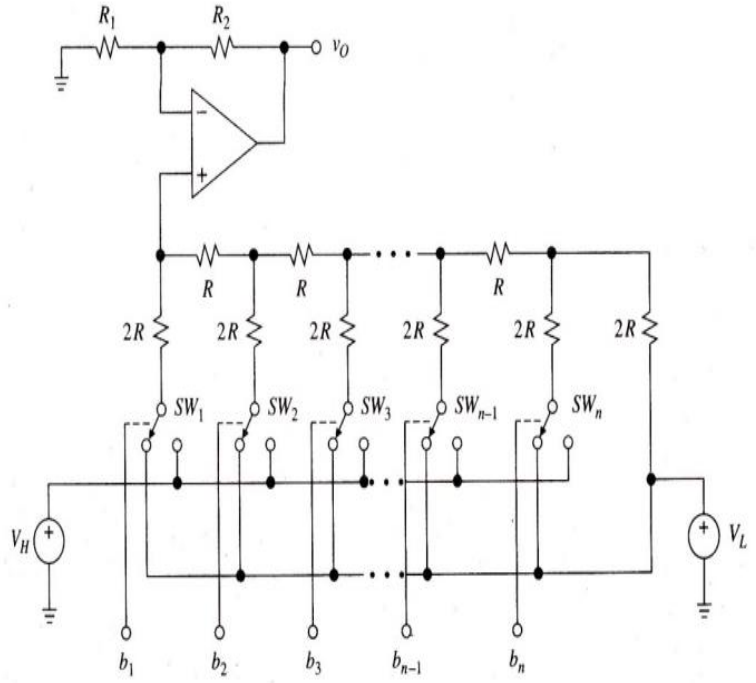
1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.

2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the

speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

VOLTAGE MODE DAC

This is the alternative mode of DAC and is called so because, the 2R resistance in the shunt path is switched between two voltages named as VL and VH. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0…..0) to all 1s (1…..1). The voltage of this node changes in steps of 2-n (VH - VL) from the minimum voltage of Vo = VL to the maximum of Vo = VH - 2-n (VH - VL).



The diagram also shows a non-inverting amplifier from which the final output is taken. Due to this buffering with a non- inverting amplifier, a scaling factor defined by $K = 1 + (R_2/R_1)$ results.

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.

2. More accurate selection and design of resistors R and 2R are possible and simple construction.

3. The binary word length can be easily increased by adding the required number or

R-2R sections.

lution

e output voltage for input 101101111 is

10.3 mV $(1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$

10.3 mV (367) = 3.78 V

ample 10.2

lculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V nge.

lution

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

For 10 V range, $$\text{LSB} = \frac{10\text{ V}}{256} = 39\text{ mV}$$

d $$\text{MSB} = \left(\frac{1}{2}\right) \text{ full scale} = 5\text{ V}$$

Full scale output = (Full scale voltage – 1 LSB)

= 10 V – 0.039 V = 9.961 V

ample 10.3

nat output voltage would be produced by a D/A converter whose output range is 0 to V and whose input binary number is

) 10 (for a 2-bit D/A converter)

) 0110 (for a 4-bit DAC)

) 10111100 (for a 8-bit DAC)

lution

) $V_o = 10\text{ V}\left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5\text{ V}$

i) $V_o = 10\text{ V}\left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right)$

$= 10\left(\frac{1}{4} + \frac{1}{8}\right) = 3.75\text{ V}$

ii) $V_o = 10\text{ V}\,(1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5$
$+ 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$
$= 10\text{ V}\,(1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34\text{ V}$

03 A-D CONVERTERS

he block schematic of ADC shown in Fig. 10.9 provides the function just opposite to that a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1 d_2 \ldots d_n$

of functional value D, so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \qquad (10.3)$$

where d_1 is the most significant bit and d_n is the least significant bit. An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and the EOC (end of conversion) output to announce when the conversion is complete. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

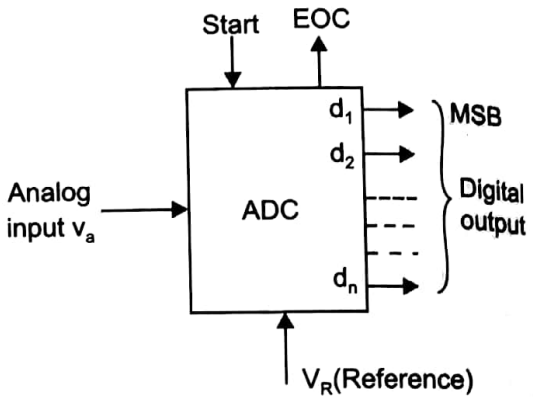


Fig. 10.9 Functional diagram of ADC

ADCs are classified broadly into two groups according to their conversion technique. Direct type ADCs and Integrating type ADCs. Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

Flash (comparator) type converter
Counter type converter
Tracking or servo converter
Successive approximation type converter

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

(i) Charge balancing ADC
(ii) Dual slope ADC

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash (comparator) type is expensive for high degree of accuracy. The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

DIRECT TYPE ADCs

10.3.1 The Parallel Comparator (Flash) A/D Converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure 10.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 10.10 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 10.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table for the flash type AD converter is shown in Fig. 10.10 (c). The circuit has the advantage of high speed as the

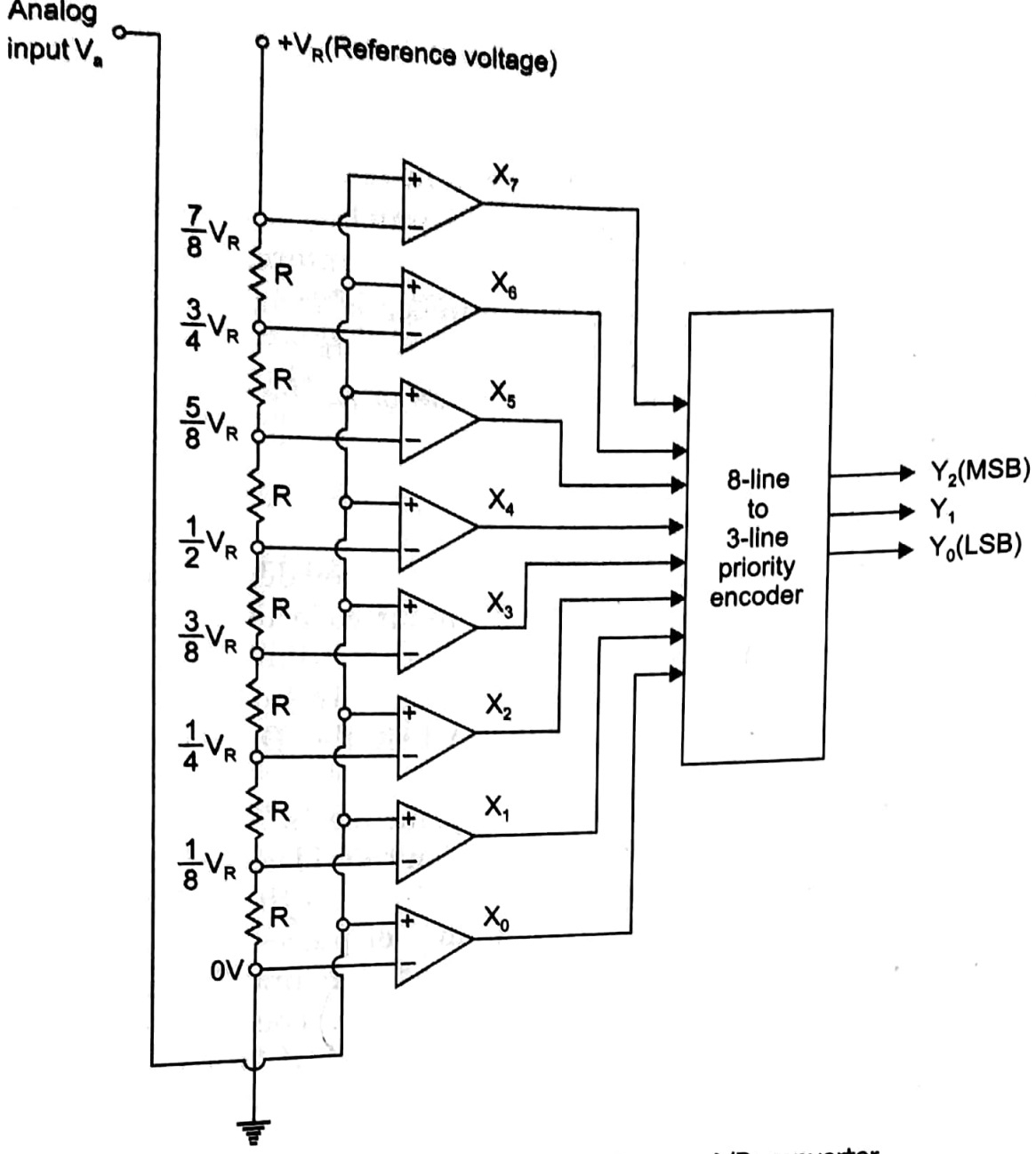


Fig. 10.10 (a) Basic circuit of a flash type A/D converter

Voltage input	*Logic output X*
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

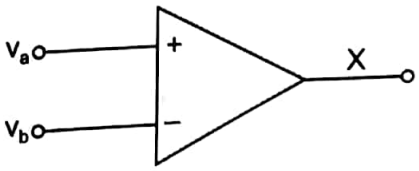


Fig. 10.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 10.10 (c) Truth table for a flash type A/D converter

conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are $2^n - 1$ where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.

10.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within ± (1/2) LSB to the analog input V_a which is to be converted to binary digital form. Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within ± (1/2) LSB to V_a.

A 3-bit counting ADC based upon the above principle is shown in Fig. 10.11 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output is a staircase of the type shown in Fig. 10.11 (b). The analog output V_d of DAC is compared to the analog input V_a by the comparator. If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When $V_a < V_d$, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a. For a new value of analog input V_a, a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again

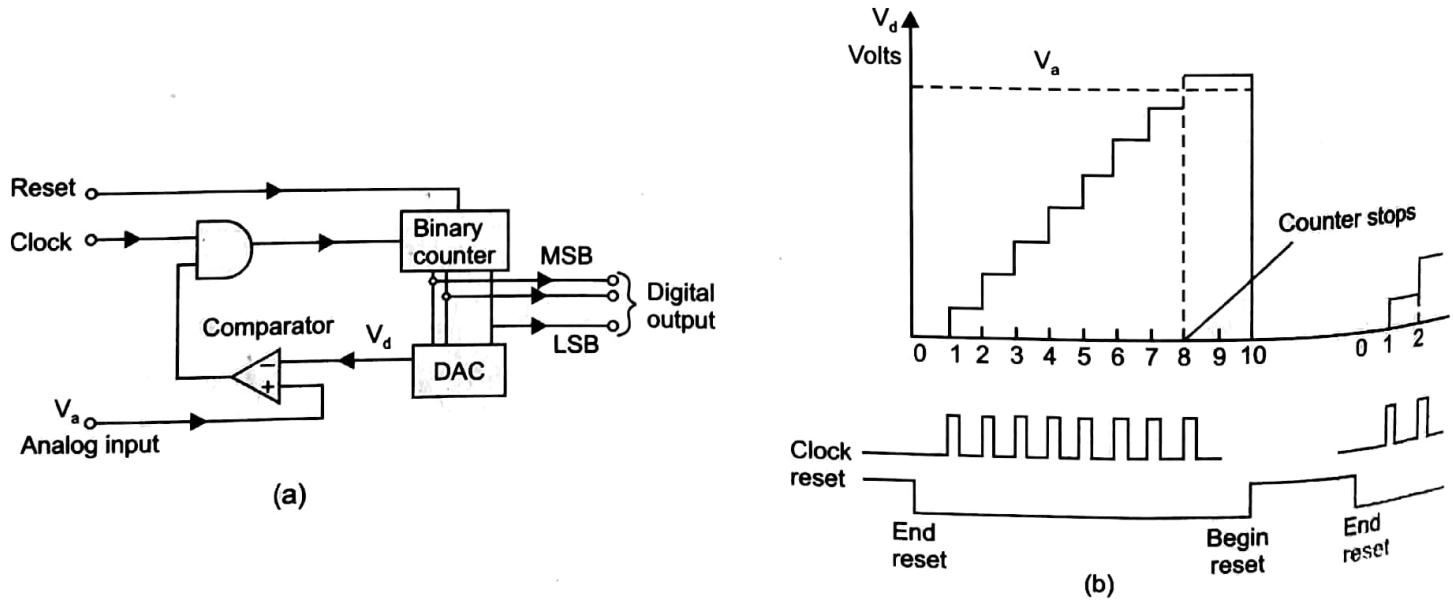


Fig. 10.11 (a) A counter type A/D converter (b) D/A output staircase waveform

as shown in Fig. 10.11 (b). The counter frequency must be low enough to give sufficient time for the DAC to settle and for the comparator to respond. Low speed is the most serious drawback of this method. The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of input voltage V_a. For instance, a 12-bit system with 1 MHz clock frequency, the counter will take $(2^{12} - 1)$ μs = 4.095 ms to convert a full scale input.

If the analog input voltage varies with time, the input signal is sampled, using a sample and hold circuit before it is applied to the comparator. If the maximum value of the analog voltage is represented by n-pulses and if the clock period is T seconds, the minimum interval between samples is nT seconds.

0.3.3 Servo Tracking A/D Converter

n improved version of counting ADC is the tracking or a servo converter shown in Fig. 0.12 (a). The circuit consists of an up/down counter with the comparator controlling the irection of the count. The analog output of the DAC is V_d and is compared with the analog nput V_a. If the input V_a is greater than the DAC output signal, the output of the comparator oes high and the counter is caused to count up. The DAC output increases with each ncoming clock pulse and when it becomes more than V_a, the counter reverses the direction nd counts down (but only by one count, LSB). This causes the control to count up and the ount increases by 1 LSB. The process goes on being repeated and the digital output changes ack and forth by ±1 LSB around the correct value. As long as the analog input changes owly, the tracking A/D will be within one LSB of the correct value. However, when the nalog input changes rapidly, the tracking A/D cannot keep up with the change and error curs as shown in Fig. 10.12 (b).

The tracking ADC has the advantage of being simple. The disadvantage, however, is the ne needed to stabilize as a new conversion value is directly proportional to the rate at nich the analog signal changes.

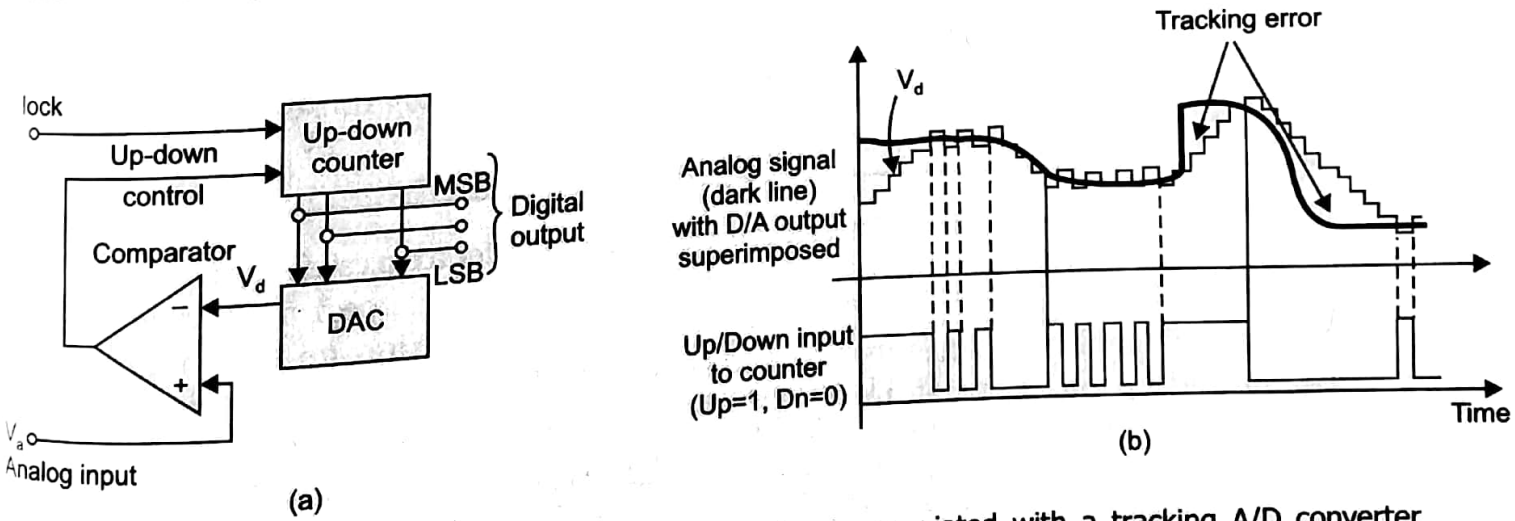


Fig. 10.12 (a) A tracking A/D converter (b) Waveforms associated with a tracking A/D converter

10.3.4 Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. Figure 10.13 shows an eight bit converter. The circuit uses a

successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now compared with analog input V_a. If V_a is greater than the DAC output V_d then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

However, if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses V_a, the comparator changes state and th can be taken as the end of conversion (EOC) command. Figure 10.14 (a) shows a typica conversion sequence and Fig. 10.14 (b

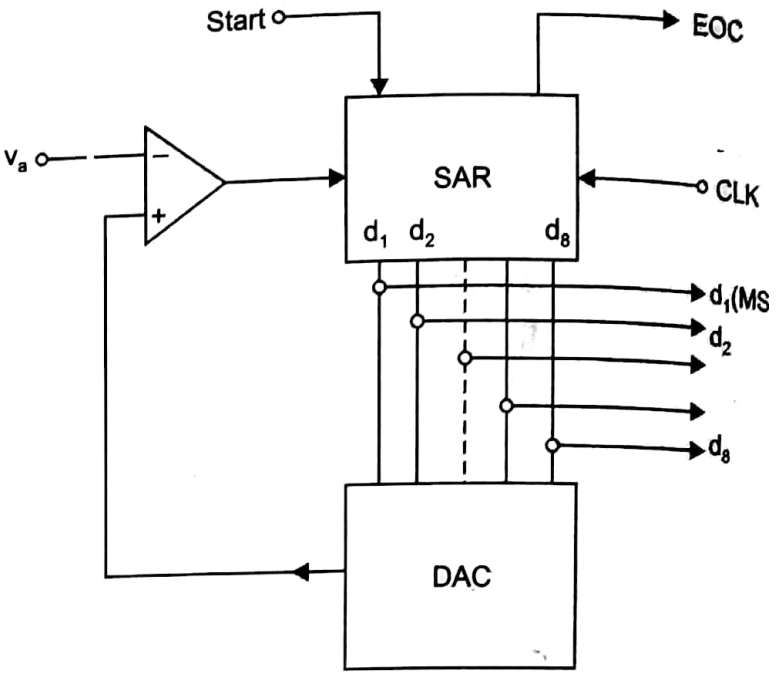


Fig. 10.13 Functional diagram of the successive approximation ADC

Correct digital representation	*Successive approximation register output V_d at different stages in conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

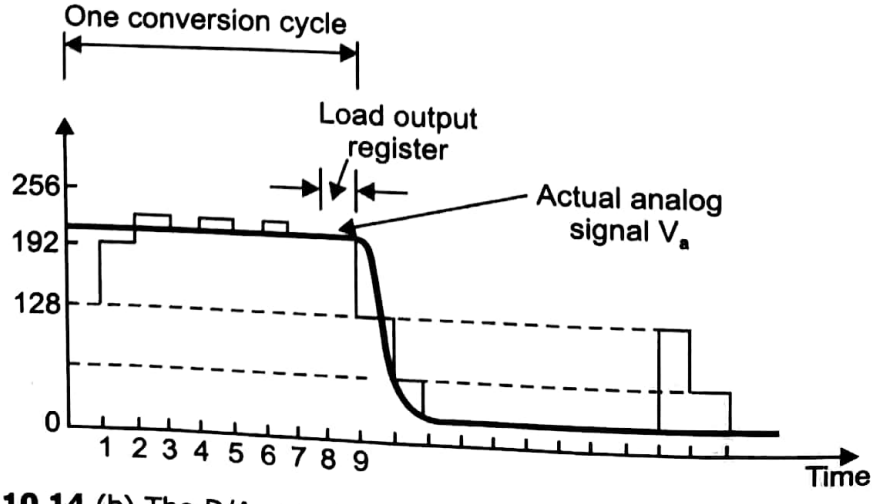


Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

shows the associated wave forms. It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 10.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far.

Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

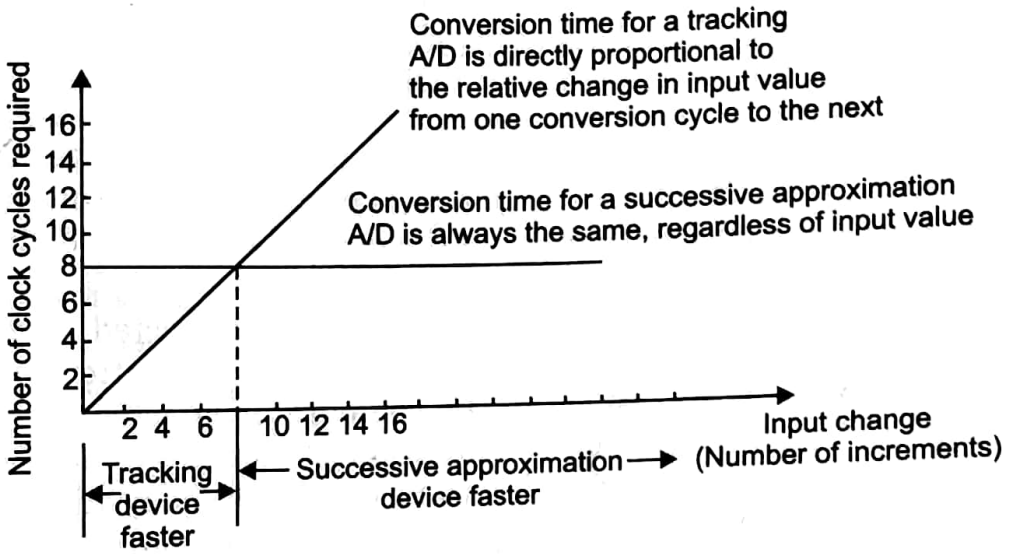


Fig. 10.15 Comparison of conversion times for tracking and successive approximation A/D devices

tegrating Type of ADCs

he integrating type of ADCs do not require a S/H circuit at the input. If the input changes uring conversion, the ADC output code will be proportional to the value of the input veraged over the integration period.

0.3.5 Charge Balancing ADC

he principle of charge balancing ADC is to first convert the input signal to a frequency sing a voltage to frequency (V/F) converter. This frequency is then measured by a counter nd converted to an output code proportional to the analog input. The main advantage of hese converters is that it is possible to transmit frequency even in noisy environment or in solated form. However, the limitation of the circuit is that the output of V/F converter depends upon an RC product whose value cannot be easily maintained with temperature and time. The drawback of the charge balancing ADC is eliminated by the dual slope conversion.

10.3.6 Dual-Slope ADC

Figure 10.16 (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator. The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods as shown in Fig. 10.16 (b). Then it integrates an internal

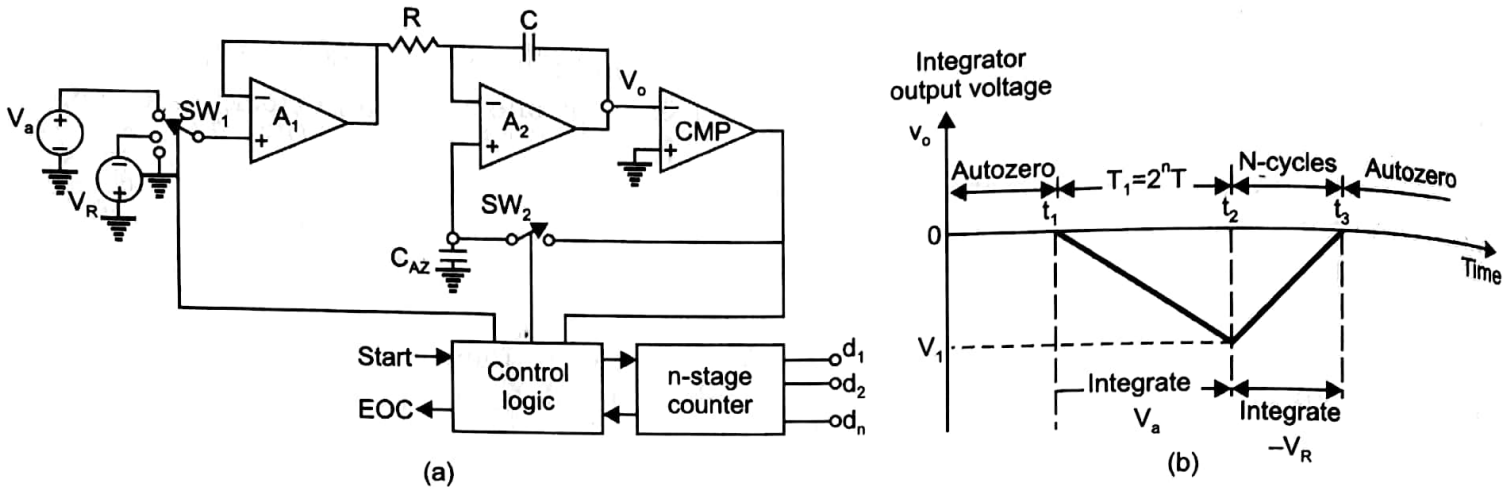


Fig. 10.16 (a) Functional diagram of the dual slope ADC (b) Integrated output waveform for the dual slope ADC

reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code. The circuit operates as follows:

Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation for the input-offset voltages of all the three amplifiers. Later, when SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in Fig. 10.16 (b).

The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage $(-V_R)$. The output voltage v_o will now have a positive slope. As long as v_o is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when v_o becomes just zero at time $t = t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog input voltage V_a.

In Fig. 10.16 (b)

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}} \tag{10.4}$$

and

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}} \tag{10.5}$$

For an integrator,

$$\Delta v_o = (-1/RC)\ V(\Delta t) \tag{10.6}$$

The voltage v_o will be equal to v_1 at the instant t_2 and can be written as

$$v_1 = (-1/RC)\, V_a(t_2 - t_1)$$

The voltage v_1 is also given by

$$v_1 = (-1/RC)\,(-V_R)\,(t_2 - t_3)$$

So,
$$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$

or,
$$V_a = (V_R)\,(N/2^n) \qquad (10.7)$$

The following important observations can be made:

1. Since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is independent of R, C and T.
2. The dual-slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T_1. Thus ac noise superimposed on the input signal such as 50 Hz power line pick-up will be averaged during the input integration time. So choose clock period T, so that 2^nT is an exact integral multiple of the line period (1/50) second = 20 ms.
3. The main disadvantage of the dual-slope ADC is the long conversion time. For instance, if $2^n - T$ = 1/50 is used to reject line pick-up, the conversion time will be 20 ms.

Dual-slope converters are particularly suitable for accurate measurement of slowly varying ignals, such as thermocouples and weighing scales. Dual-slope ADCs also form the basis of igital panel meters and multimeters.

Dual-slope converters are available in monolithic form and are available both in icroprocessor compatible and in display oriented versions. The former provide the digital ode in binary form whereas the display oriented versions present the output code in a rmat suitable for the direct drive of LED displays. The Datel Intersil ICL7109 is a monolithic 2-bit dual-slope ADC with microprocessor compatibility.

xample 10.4

A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10 V. The maximum integrator output voltage should be – 8 V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μF. Find the value of the resistor R of the integrator.

Solution

Time period $(t_2 - t_1)$ in Fig. 10.16 (b) $= \dfrac{2^{16}}{4\text{ MHz}} = \dfrac{65536}{4\text{ MHz}} = 16.38$ ms

For the integrator

$$\Delta v_o = (-1/RC)\, V_a(t_2 - t_1)$$

So,
$$RC = -(10\text{ V}/-8\text{ V})\ 16.3\text{ ms} = 20.47\text{ ms}$$

$$R = \frac{20.47\text{ ms}}{0.1\,\mu\text{F}} = 204.7\text{ k}\Omega = 205\text{ k}\Omega$$

Example 10.5

If the analog signl V_a is +4.129 V in the example 10.4, find the equivalent digital number.

Solution

Since, $V_a = V_R(N/2^n)$

So the digital count $N = 2^n\ (V_a/V_R) = 65536\ (4.129\ V/8\ V) = 33825$ for which the binary equivalent is 1000010000100001.

10.4 DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed.

Resolution: The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has $2^8-1 = 255$ equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1\ \text{LSB increment} \tag{10.8}$$

However, resolution is stated in a number of different ways. An 8-bit DAC is said to have
: 8 bit resolution
: a resolution of 0.392 of full-scale
: a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table 10.1 gives the resolution for 6–16 bit DACs.

Table 10.1 Resolution for 6-16 bit DACs

Bits	*Intervals*	*LSB size (% of Full Scale)*	*LSB size (10 V Full Scale)*
6	63	1.588	158.8 mV
8	256	0.392	39.2 mV
10	1023	0.0978	9.78 mV
12	4095	0.0244	2.44 mV
14	16383	0.0061	0.61 mV
16	65535	0.0015	0.15 mV

Linearity: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 10.17. The static performance of a DAC is determined by

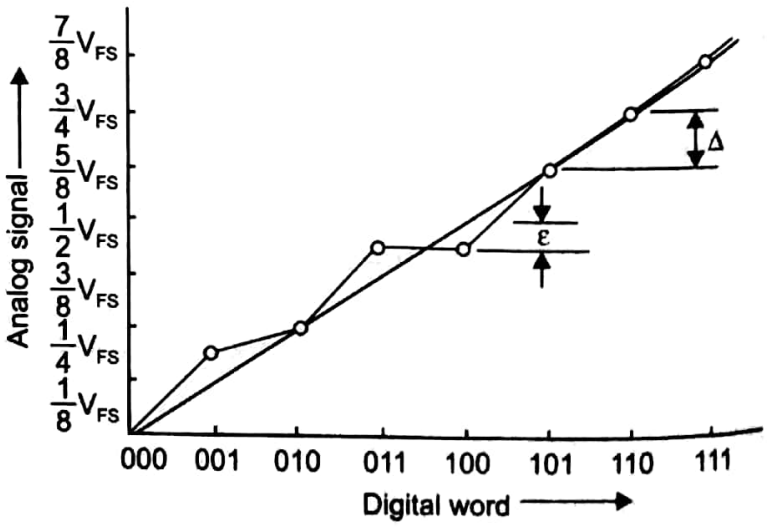


Fig. 10.17 Linearity error for 3-bit DAC

fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted line and is given by ε/Δ as shown in Fig. 10.17. The error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ± (1/2) LSB.

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specify relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

Monotonicity: A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure 10.18 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes.

If a DAC has to be monotonic, the error should be less than ±(1/2) LSB at each output level. All the commercially available DACs are monotonic because the linearity error never exceeds ±(1/2) LSB at each output level.

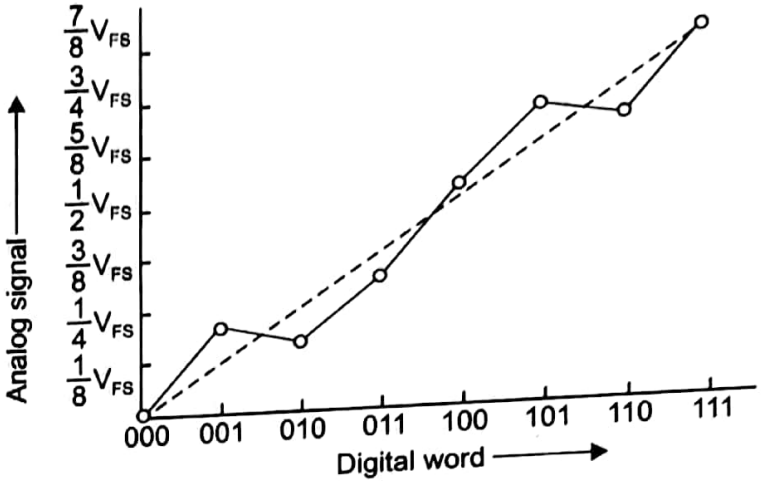


Fig. 10.18 A non-monotonic 3-bit DAC

Settling time: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ±(1/2) LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Stability: The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

A brief overview of ADC and DAC selection guide is given below:

A/D converters:	
AD 7520/AD 7530	10-bit binary multiplying type
AD 7521/AD 7531	12-bit binary multiplying type
ADC 0800/0801/0802	8-bit ADC
D/A converters:	
DAC 0800/0801/0802	8-bit DAC
DAC 0830/0831/0832	microprocessor compatible 8-bit DAC
DAC 1200/1201	12-bit DAC
DAC 1208/1209/1210	12-bit microprocessor compatible DAC