Op-amp Applications:

SUMMING, SCALING, AND AVERAGING AMPLIFIERS

Inverting Configuration

Figure shows the inverting configuration with three inputs *Va, Vb,* and *Vc.* Depending on the relationship between the feedback resistor R_f and the input resistors *Ra, Rb,* and *Rc,* the circuit can be used as either a summing amplifier, scaling amplifier, or averaging amplifier. The circuit's function can be verified by examining the expression for the output voltage *V0,* which is obtained from Kirchhoff's current equation written at node *V2.* Referring to Figure

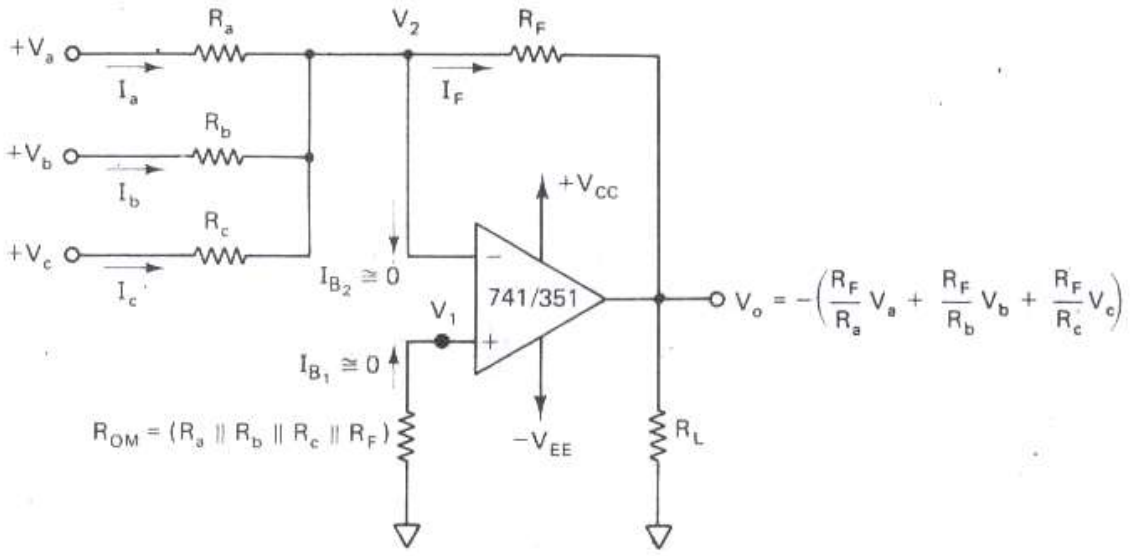


Figure Inverting configuration with three inputs can be used as a summing amplifier, scaling amplifier, or averaging amplifier.

$$I_a + I_b + I_c = I_B + I_F$$

Since R_i and A of the op-amp are ideally infinity, $I_B = 0$ A and $V_1 = V_2 \cong 0$ V. Therefore,

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_F}$$

or

$$V_o = -\left(\frac{R_F}{R_a} V_a + \frac{R_F}{R_b} V_b + \frac{R_F}{R_c} V_c\right)$$

Summing amplifier.

If Ra=Rb=Rc=R then

$$V_o = -\frac{R_F}{R}(V_a + V_b + V_c)$$

This means that the output voltage is equal to the *negative* sum of all the inputs times the gain of the circuit R_F/R; hence the circuit is called a *summing amplifier*. Obviously, when the gain of the circuit is 1, that is, $R_a = R_b = R_c = R_F$, the output voltage is equal to the *negative* sum of all input voltages. Thus

$$V_o = -(V_a + V_b + V_c)$$

Scaling or weighted amplifier. If each input voltage is amplified by a different factor, in other words, weighted differently at the output, the circuit in Figure is then called a *scaling* or *weighted amplifier*. This condition can be accomplished if R_a, R_b, and R_c are different in value. Thus the output voltage of the scaling amplifier is

$$V_o = -\left(\frac{R_F}{R_a} V_a + \frac{R_F}{R_b} V_b + \frac{R_F}{R_c} V_c\right)$$

where

$$\frac{R_F}{R_a} \neq \frac{R_F}{R_b} \neq \frac{R_F}{R_c}$$

Average circuit.

The circuit of Figure can be used as an *averaging circuit*, in which the output voltage is equal to the average of all the input voltages. This is accomplished by using all input resistors of equal value, $R_a = R_b = R_c = R$. In addition, the gain by which each input is amplified must be equal to 1 over the number of inputs; that is,

$$\frac{R_F}{R} = \frac{1}{n}$$

where n is the number of inputs.

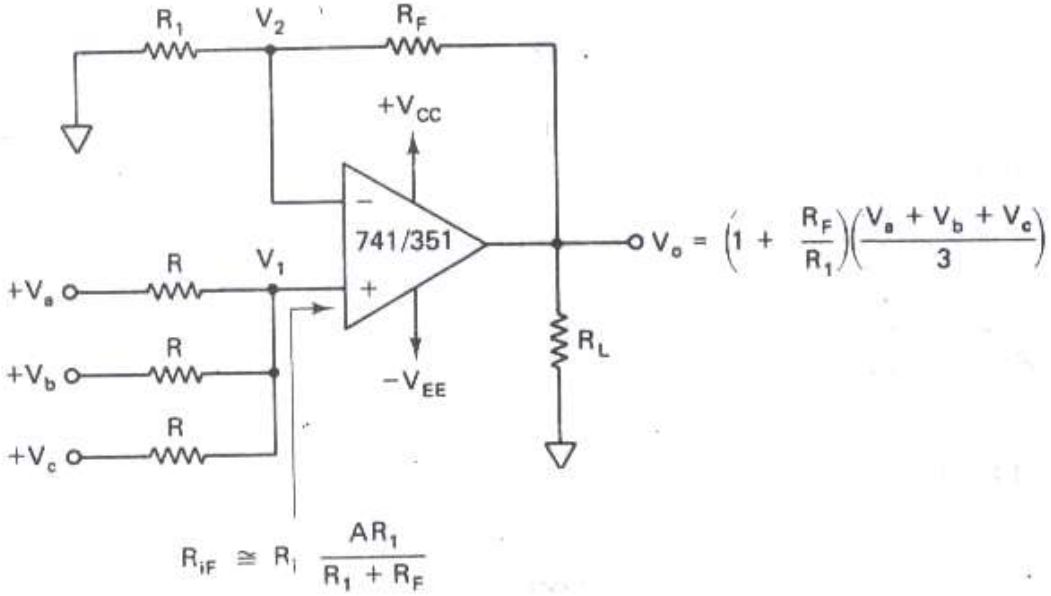
Noninverting Configuration

Again, to verify the functions of the circuit, the expression for the output voltage must be obtained. Recall that the input resistance R_{iF} of the noninverting amplifier is very large (see Figure . Therefore, using the superposition theorem, the voltage V_1 at the noninverting terminal is

$$V_1 = \frac{R/2}{R + R/2} V_a + \frac{R/2}{R + R/2} V_b + \frac{R/2}{R + R/2} V_c$$

or

$$V_1 = \frac{V_a}{3} + \frac{V_b}{3} + \frac{V_c}{3} = \frac{V_a + V_b + V_c}{3}$$



Hence the output voltage V_o is

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1$$

$$= \left(1 + \frac{R_F}{R_1}\right) \frac{V_a + V_b + V_c}{3}$$

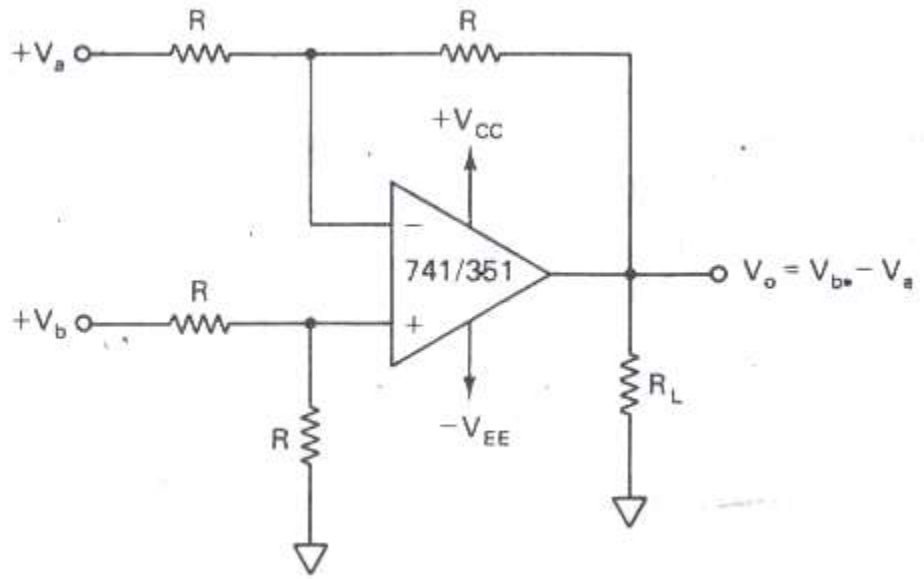
Averaging amplifier. If $(1+R_F/R_1)=1$; It will be averaging amplifier.

Summing amplifier. If $(1+R_F/R_1)=3$; It will be summing amplifier.

Scaling or weighted amplifier. It is basically scaling amplifier.

Differential Configuration

A subtractor.



From this figure, the output voltage of the differential amplifier with a gain of 1 is

$$V_o = -\frac{R}{R}(V_a - V_b)$$

That is,

$$V_o = V_b - V_a$$

INSTRUMENTATION AMPLIFIER

In many industrial and consumer applications the measurement and control of physical conditions are very important. For example, measurements of temperature and humidity inside a dairy or meat plant permit the operator to make necessary adjustments to maintain product quality. Similarly, precise temperature control of a plastic furnace is needed to produce a particular type of plastic.

Generally, a transducer is used at the measuring site to obtain the required information easily and safely. The *transducer* is a device that converts one form of energy into another.

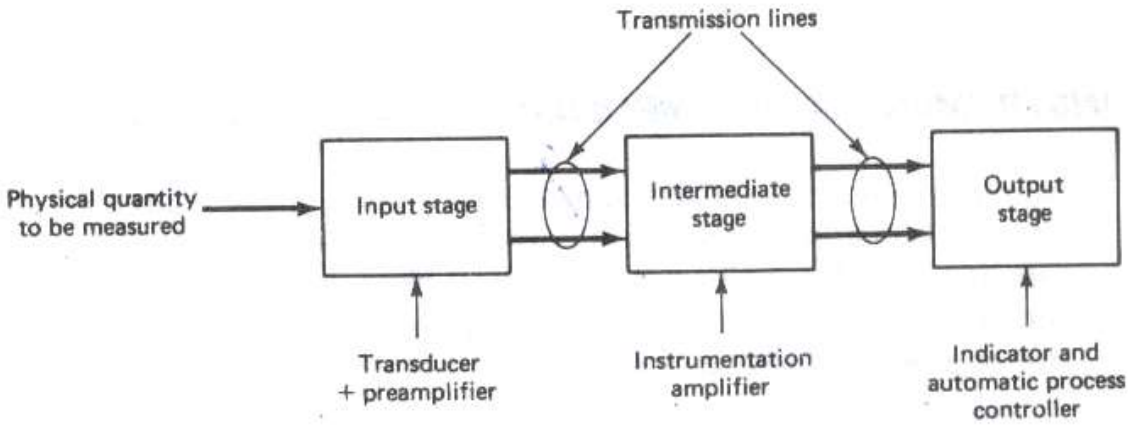
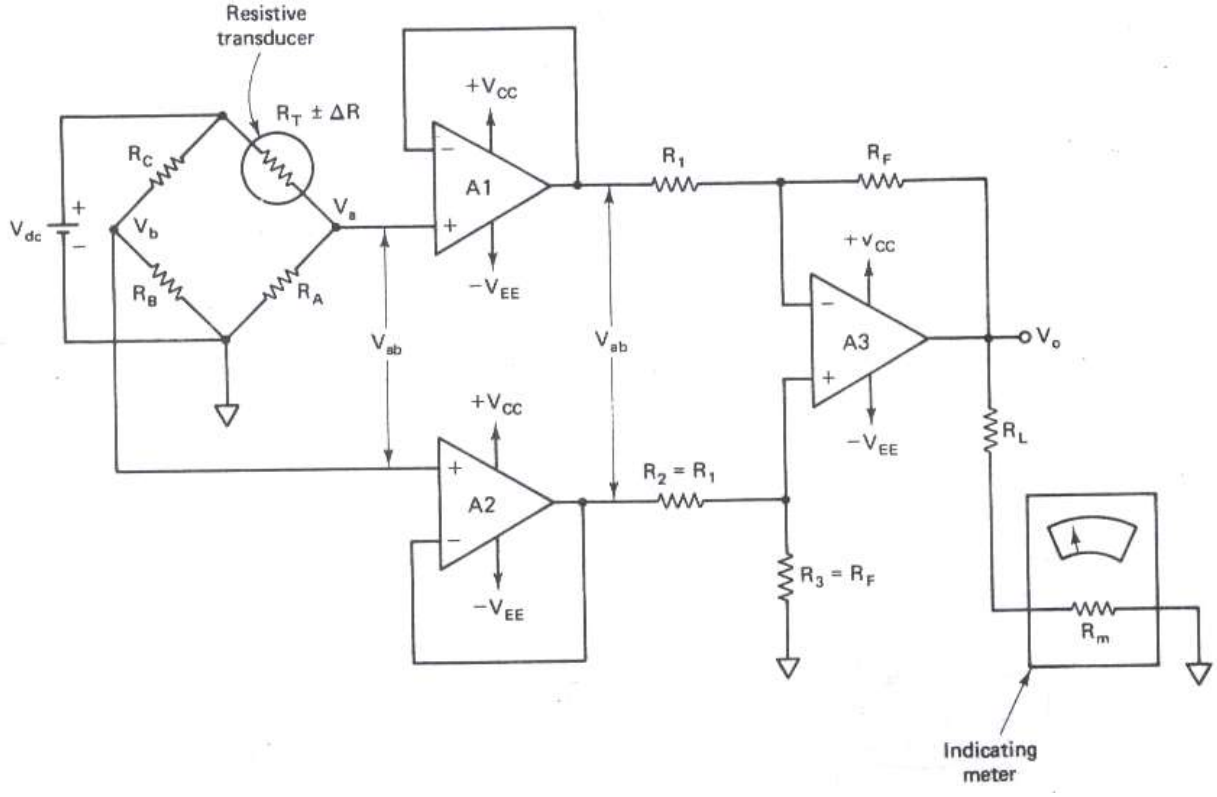


Figure 7–11 Block diagram of an instrumentation system.

An instrumentation system is used to measure the output signal produced by a transducer and often to control the physical signal producing it.

The input stage is composed of a preamplifier and some sort of transducer, depending on the physical quantity to be measured. The output stage may use devices such as meters, oscilloscopes, charts, or magnetic recoders.

Instrumentation Amplifier Using Transducer Bridge



A *resistive transducer* whose resistance changes as a function of some physical energy is connected in one arm of the bridge with a small circle around it and is denoted by $(R_T \pm \Delta R)$, where R_T is the resistance of the transducer and ΔR the change in resistance R_T.

The bridge in the circuit of Figure is dc excited but could be ac excited as well. For the balanced bridge at some reference condition,

$$V_b = V_a$$

or

$$\frac{R_B(V_{dc})}{R_B + R_C} = \frac{R_A(V_{dc})}{R_A + R_T}$$

That is,

$$\frac{R_C}{R_B} = \frac{R_T}{R_A}$$

The bridge is balanced initially at a desired reference condition. However, as the physical quantity to be measured changes, the resistance of the transducer also changes, which causes the bridge to unbalance ($V_a \neq V_b$). The output voltage of the bridge can be expressed as a function of the change in resistance of the transducer, as described next.

Let the change in resistance of the transducer be ΔR. Since R_B and R_C are fixed resistors, the voltage V_b is constant. However, voltage V_a varies as a function of the change in transducer resistance. Therefore, according to the voltage-divider rule,

$$V_a = \frac{R_A(V_{dc})}{R_A + (R_T + \Delta R)}$$

$$V_b = \frac{R_B(V_{dc})}{R_B + R_C}$$

Consequently, the voltage V_{ab} across the output terminals of the bridge is

$$V_{ab} = V_a - V_b$$

$$= \frac{R_A V_{dc}}{R_A + R_T + \Delta R} - \frac{R_B V_{dc}}{R_B + R_C}$$

However, if $R_A = R_B = R_C = R_T = R$, then

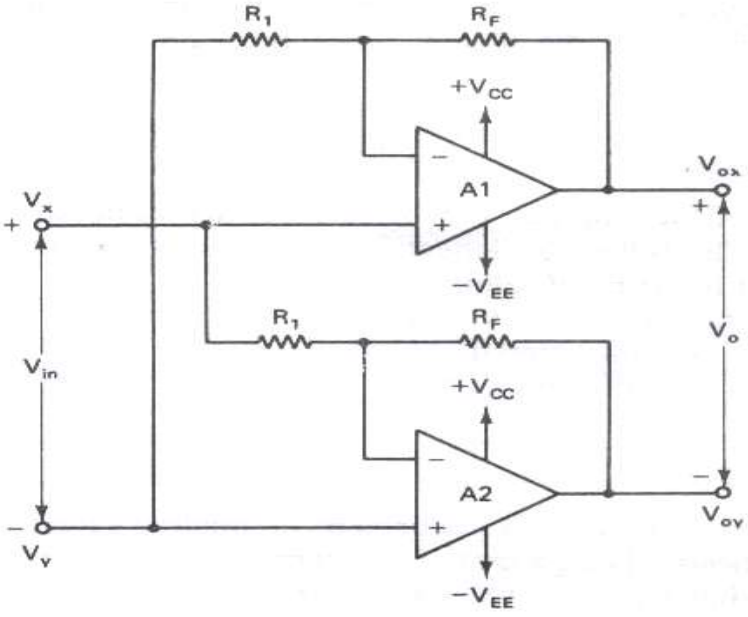
$$V_{ab} = -\frac{\Delta R(V_{dc})}{2(2R + \Delta R)}$$

The negative (−) sign in this equation indicates that $V_a < V_b$ because of the increase in the value of R_T.

The output voltage V_{ab} of the bridge is then applied to the differential instrumentation amplifier composed of three op-amps (see Figure). The voltage followers preceding the basic differential amplifier help to eliminate loading of the bridge circuit. The gain of the basic differential amplifier is $(-R_F/R_1)$; therefore, the output V_o of the circuit is

$$V_o = V_{ab}\left(-\frac{R_F}{R_1}\right) = \frac{(\Delta R)V_{dc}}{2(2R + \Delta R)}\frac{R_F}{R_1}$$

DIFFERENTIAL INPUT AND DIFFERENTIAL OUTPUT AMPLIFIER



superposition theorem, the output V_{ox} due to inputs V_x and V_y is

$$V_{ox} = \left(1 + \frac{R_F}{R_1}\right) V_x - \left(\frac{R_F}{R_1}\right) V_y$$

Similarly, the output V_{oy} is

$$V_{oy} = \left(1 + \frac{R_F}{R_1}\right) V_y - \left(\frac{R_F}{R_1}\right) V_x$$

However, the differential output V_o is

$$V_o = V_{ox} - V_{oy}$$

Therefore, from Equations (7-18a) and (7-18b),

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_x - \left(\frac{R_F}{R_1}\right) V_y - \left(1 + \frac{R_F}{R_1}\right) V_y + \left(\frac{R_F}{R_1}\right) V_x$$

$$= \left(1 + \frac{2R_F}{R_1}\right) (V_x - V_y)$$

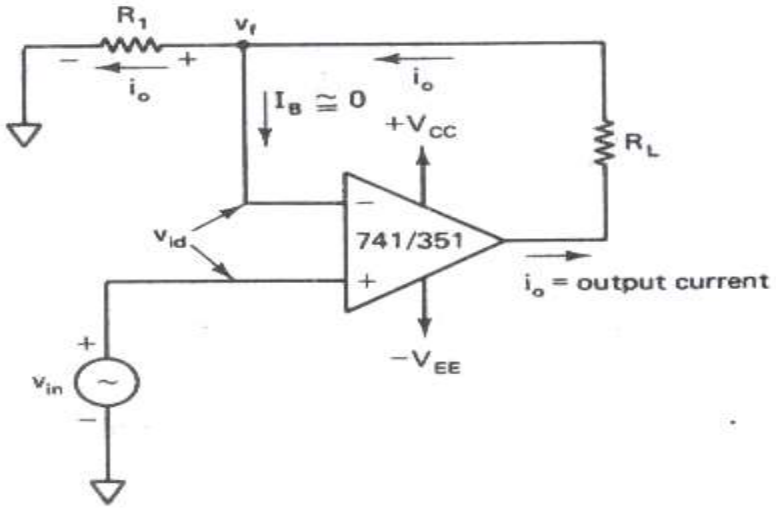
or

$$V_o = \left(1 + \frac{2R_F}{R_1}\right) V_{\text{in}}$$

This means that the differential input and output are in phase or of the same polarity provided that $V_{\text{in}} = V_x - V_y$ and $V_o = V_{ox} - V_{oy}$.

VOLTAGE-TO-CURRENT CONVERTER WITH FLOATING LOAD

Figure shows a voltage-to-current converter in which load resistor R_L is *floating* (not connected to ground). The input voltage is applied to the noninverting input terminal, and the feedback voltage across R_1 drives the inverting input terminal. This circuit is also called a *current-series negative feedback* amplifier because the feedback voltage across R_1 (applied to the inverting terminal) depends on the output current i_o and is in series with the input difference voltage v_{id}.



Writing Kirchhoff's voltage equation for the input loop,

$$v_{in} = v_{id} + v_f$$

But $v_{id} \cong 0$ V, since A is very large; therefore,

$$v_{in} = v_f$$

$$v_{in} = R_1 i_o$$

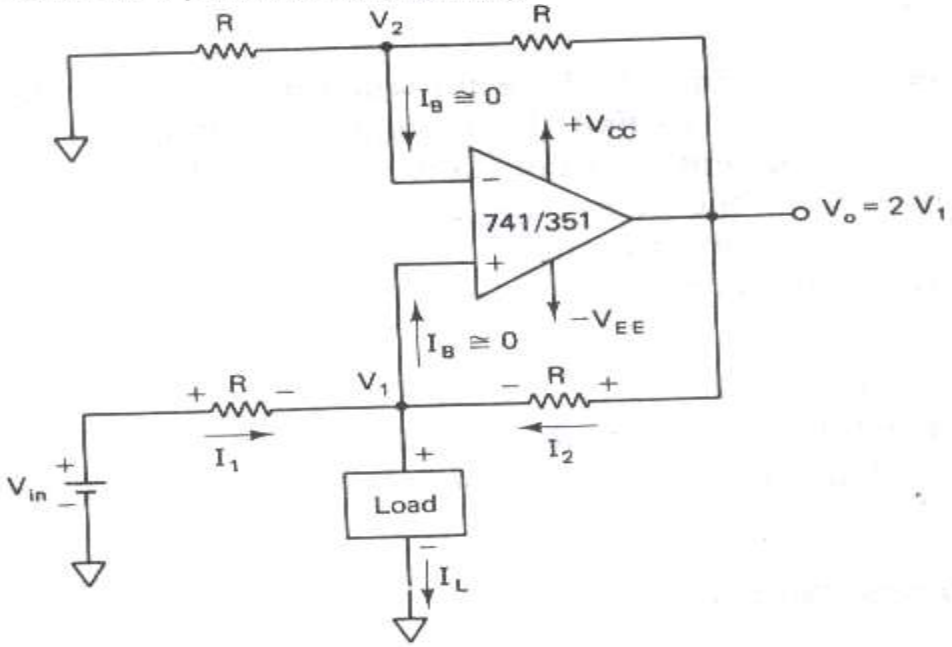
or

$$i_o = \frac{v_{in}}{R_1}$$

The voltage-to-current converter can be used in such applications as low-voltage dc and ac voltmeters, diode match finders, light-emitting diodes (LEDs), and zener diode testers.

VOLTAGE-TO-CURRENT CONVERTER WITH GROUNDED LOAD

The analysis of the circuit is accomplished by first determining the voltage V_1 at the noninverting input terminal and then establishing the relationship between V_1 and the load current.



Writing Kirchhoff's current equation at node V_1,

$$I_1 + I_2 = I_L$$

$$\frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R} = I_L$$

$$V_{in} + V_o - 2V_1 = I_L R$$

Therefore,

$$V_1 = \frac{V_{in} + V_o - I_L R}{2}$$

Since the op-amp is connected in the noninverting mode, the gain of the circuit in Figure is $1 + R/R = 2$. Then the output voltage is

$$V_o = 2V_1$$

$$= V_{in} + V_o - I_L R$$

That is,

$$V_{in} = I_L R$$

or

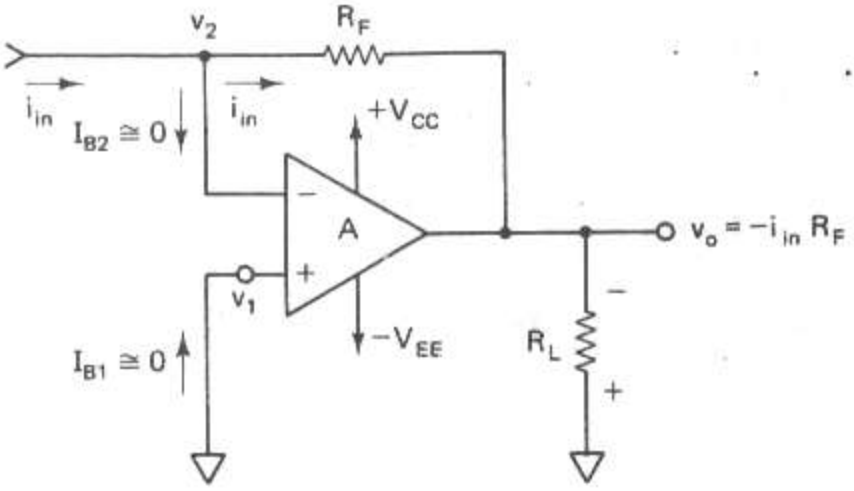
$$I_L = \frac{V_{in}}{R}$$

This means that the load current depends on the input voltage V_{in} and resistor R. Notice that all resistors must be equal in value.

The voltage-to-current converter of Figure 7-19 may also be used in testing such devices as zeners and LEDs forming a ground load. However, the circuit will perform satisfactorily provided that load size $\leq R$ value.

CURRENT-TO-VOLTAGE CONVERTER

the current-to-voltage (I-to-V) converter was presented as a special case of the inverting amplifier in which an input current is converted into a proportional output voltage. One of the most common uses of the current-to-voltage converter is in digital-to-analog circuits (DACs) and in sensing current through photodetectors such as photocells, photodiodes, and photovoltaic cells. Photosensitive devices produce a current that is proportional to an incident radiant energy or light and therefore can be used to detect the light.



Let us reconsider the ideal voltage-gain Equation of the inverting amplifier,

$$\frac{v_o}{v_{in}} = -\frac{R_F}{R_1}$$

Therefore,

$$v_o = -\left(\frac{v_{in}}{R_1}\right)R_F$$

However, since $v_1 = 0$ V and $v_1 = v_2$.

$$\frac{v_{in}}{R_1} = i_{in}$$

and

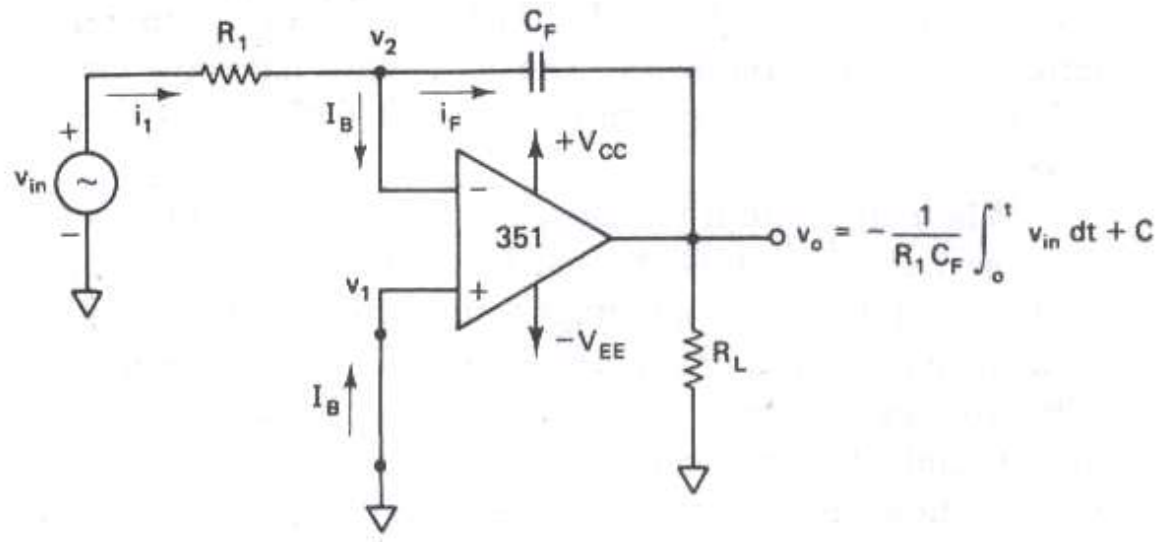
$$v_o = -i_{in}R_F$$

THE INTEGRATOR

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the *integrator* or the *integration amplifier*. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F

The expression for the output voltage v_o can be obtained by writing Kirchhoff's current equation at node v_2:

$$i_1 = I_B + i_F$$



Since I_B is negligibly small,

$$i_1 \cong i_F$$

Recall that the relationship between current through and voltage across the capacitor is

$$i_c = C\frac{dv_c}{dt}$$

Therefore,

$$\frac{v_{in} - v_2}{R_1} = C_F\left(\frac{d}{dt}\right)(v_2 - v_o)$$

However, $v_1 = v_2 \cong 0$ because A is very large. Therefore,

$$\frac{v_{in}}{R_1} = C_F\frac{d}{dt}(-v_o)$$

The output voltage can be obtained by integrating both sides with respect to time:

$$\int_0^t \frac{v_{in}}{R_1}\,dt = \int_0^t C_F\frac{d}{dt}(-v_o)\,dt$$

$$= C_F(-v_o) + v_o|_{t=0}$$

Therefore,

$$v_o = -\frac{1}{R_1C_F}\int_0^t v_{in}\,dt + C$$

where C is the integration constant and is proportional to the value of the output voltage v_o at time $t = 0$ seconds.

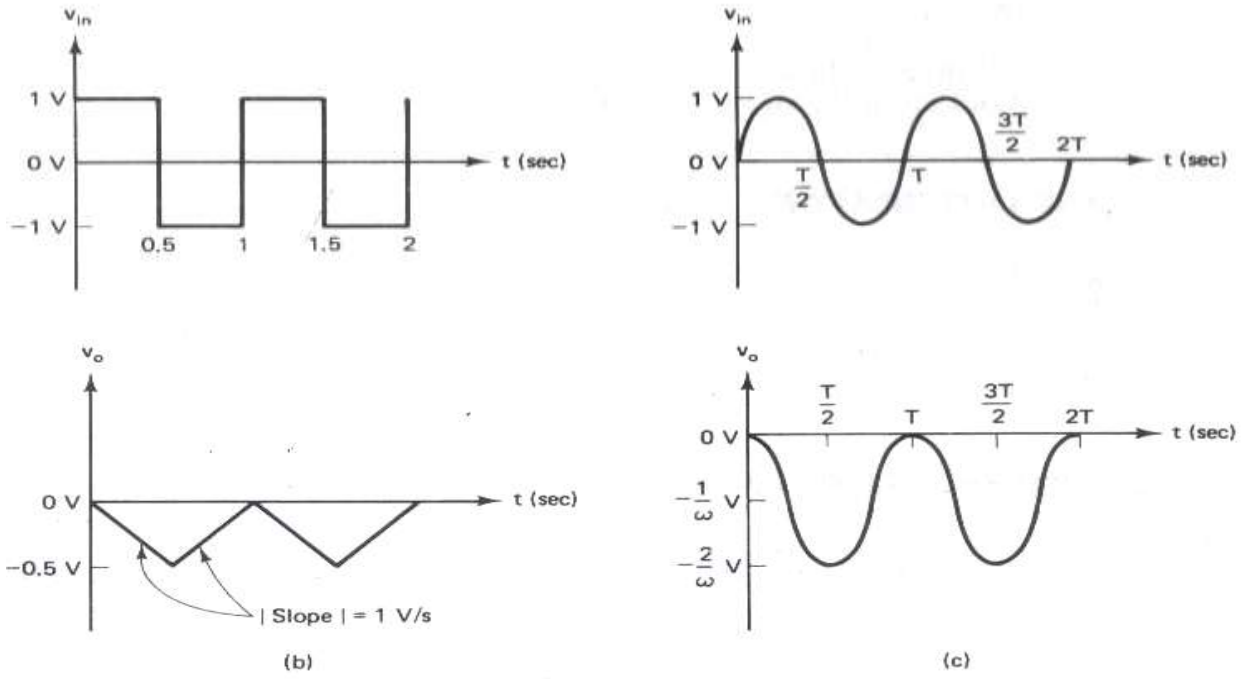


Figure (a) The integrator circuit. (b) and (c) Input and ideal output waveforms using a sine wave and square wave, respectively. $R_1C_F = 1$ second and $V_{ooT} = 0$ V assumed.

When $v_{in} = 0$, the integrator of Figure works as an open-loop amplifier. This is because the capacitor C_F acts as an open circuit ($X_{CF} = \infty$) to the input offset voltage V_{io}. In other words, the input offset voltage V_{io} and the part of the input current charging capacitor C_F produce the error voltage at the output of the integrator. Therefore, in the practical integrator shown in Figure , to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F. Thus, R_F limits the low-frequency gain and hence minimizes the variations in the output voltage.

The frequency response of the basic integrator is shown in Figure . In this figure, f_b is the frequency at which the gain is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

Both the stability and the low-frequency roll-off problems can be corrected by the addition of a resistor R_F as shown in the *practical integrator* of Figure The frequency response of the practical integrator is shown in Figure by a dashed line. In this figure, f is some relative operating frequency, and for frequencies f to f_a the gain R_F/R_1 is constant. However, after f_a the gain decreases at a rate of 20 dB/decade. In other words, between f_a and f_b the circuit of Figure acts as an integrator. The gain-limiting frequency f_a is given by

$$f_a = \frac{1}{2\pi R_F C_F}$$

Generally, the value of f_a and in turn R_1C_F and R_FC_F values should be selected such that $f_a < f_b$. For example, if $f_a = f_b/10$, then $R_F = 10R_1$.

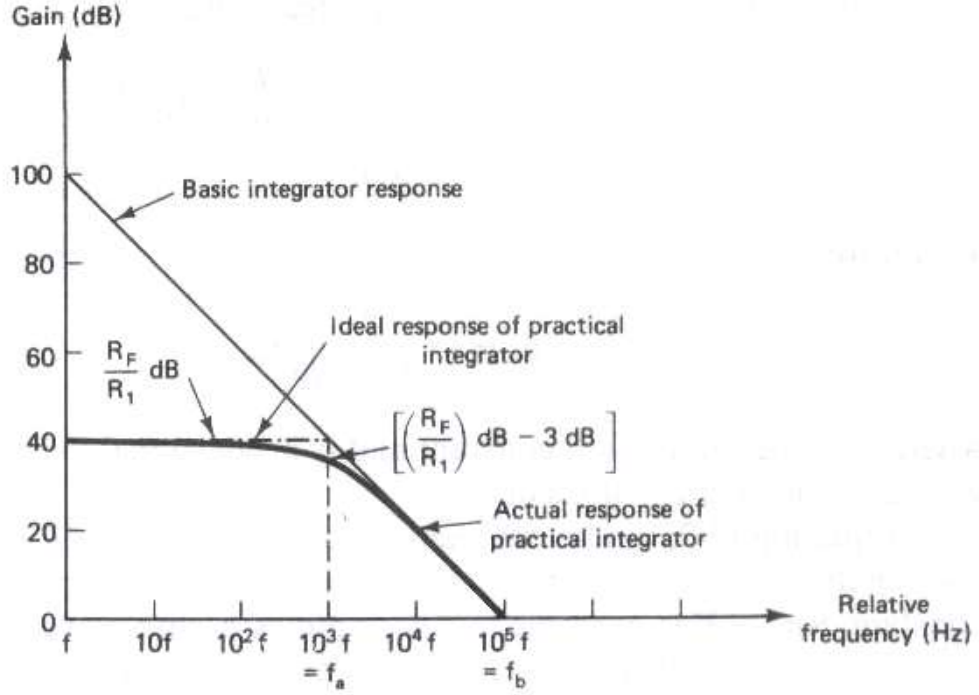


Figure Frequency response of basic and practical integrators. $f_a = 1/(2\pi R_FC_F)$ and $f_b = 1/(2\pi R_1C_F)$.

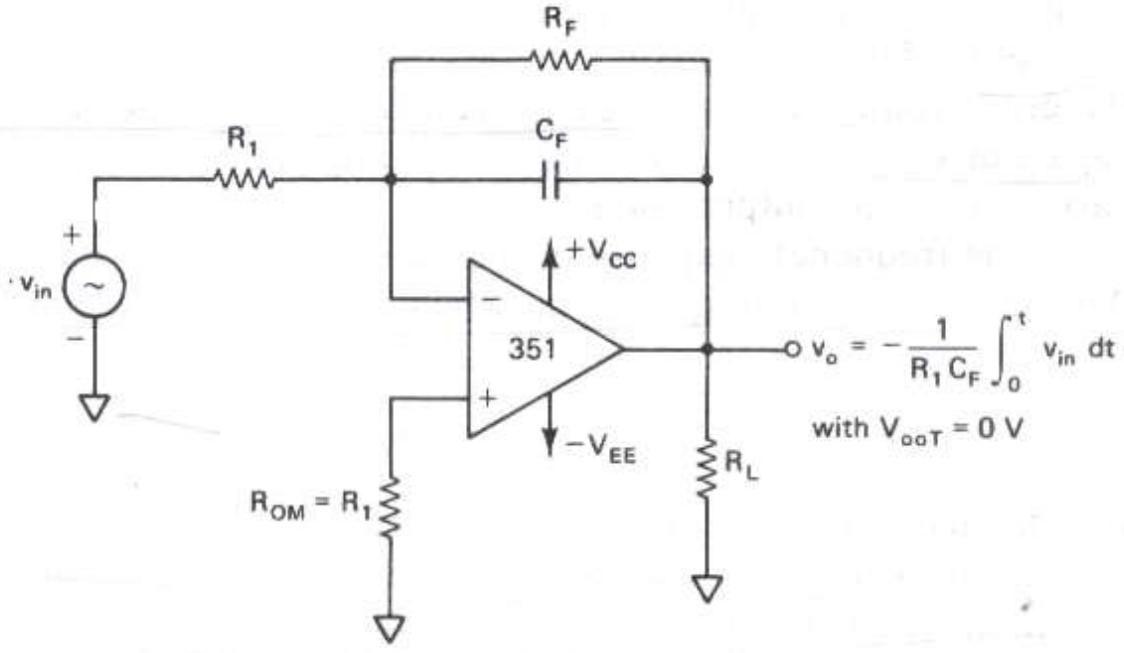


Figure Practical integrator.

input signal will be integrated properly if the time period T of the signal is larger than or equal to $R_F C_F$. That is,

$$T \geq R_F C_F$$

where

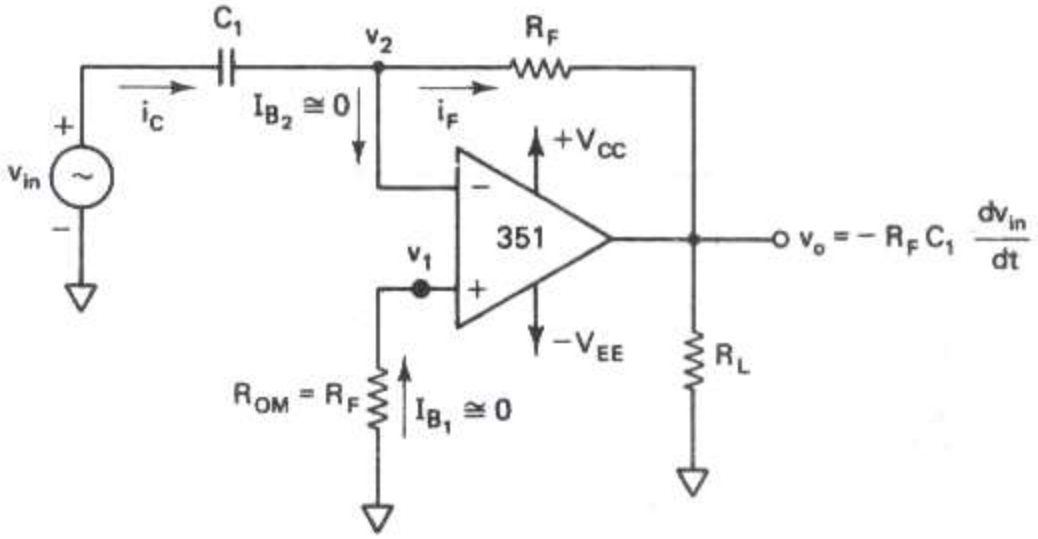
$$R_F C_F = \frac{1}{2\pi f_a}$$

THE DIFFERENTIATOR

Figure shows the *differentiator* or *differentiation amplifier*. As its name implies, the circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1.

The expression for the output voltage can be obtained from Kirchhoff's current equation written at node v_2 as follows:

$$i_C = i_B + i_F$$



(a)

Since $I_B \cong 0$,

$$i_C = i_F$$

$$C_1 \frac{d}{dt}(v_{in} - v_2) = \frac{v_2 - v_o}{R_F}$$

But $v_1 = v_2 \cong 0$ V, because A is very large. Therefore,

$$C_1 \frac{dv_{in}}{dt} = -\frac{v_o}{R_F}$$

or

$$v_o = -R_F C_1 \frac{dv_{in}}{dt}$$

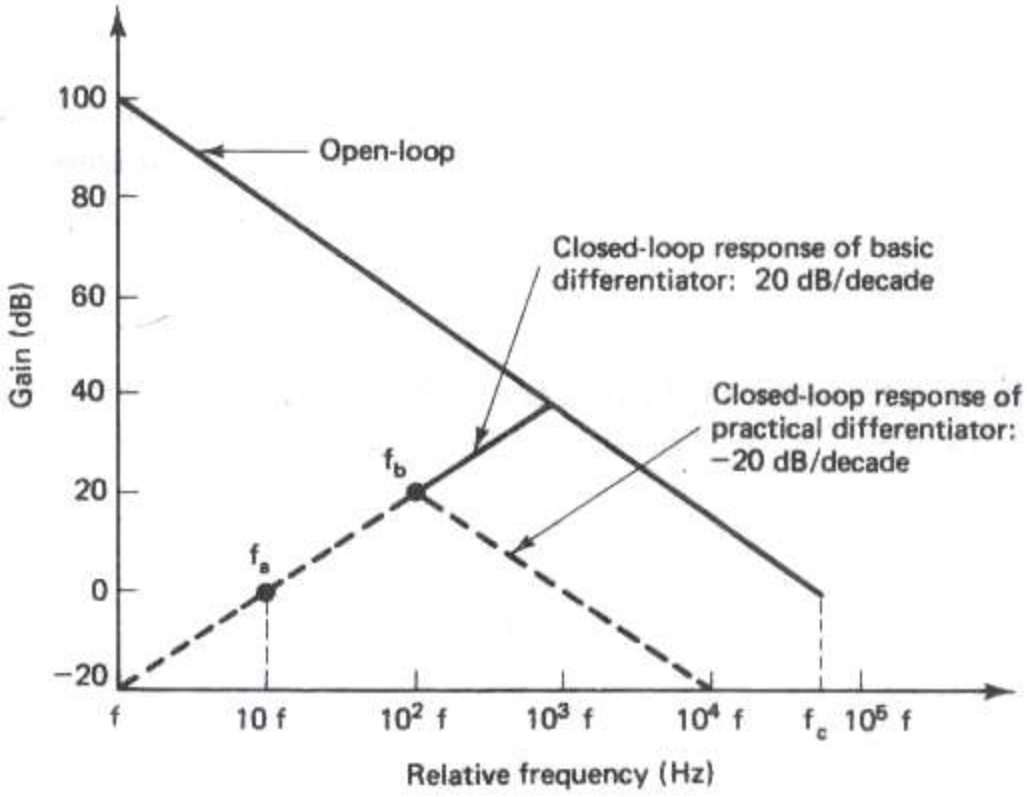
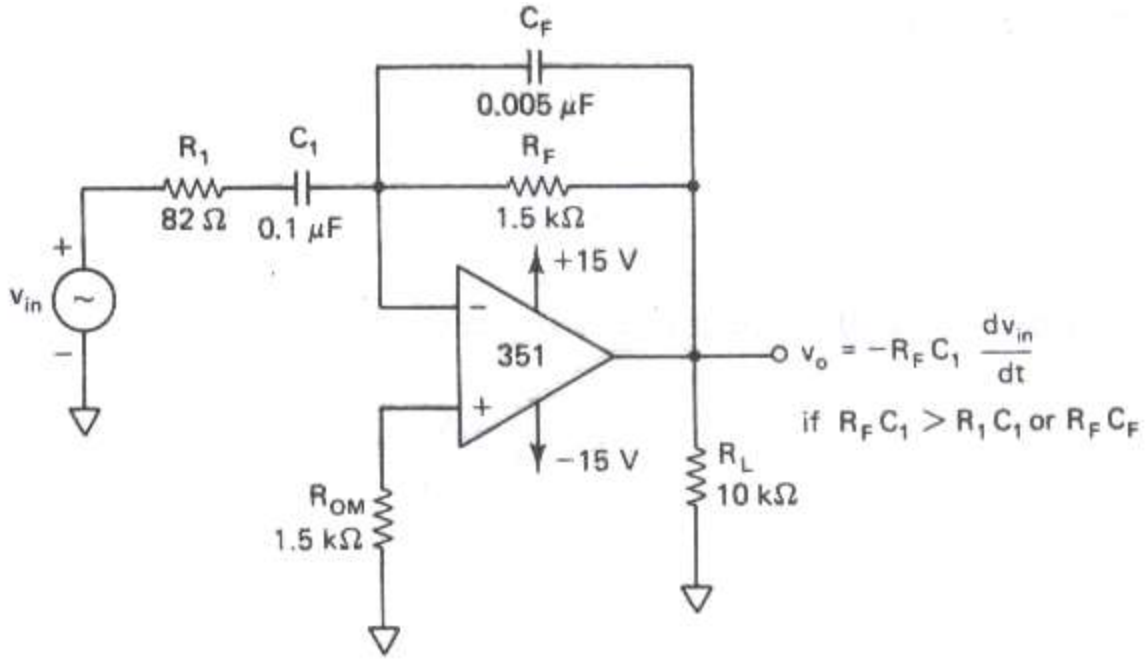


Figure Basic differentiator. (a) Circuit. (b) Frequency response.

The gain of the circuit (R_F/X_{C1}) increases with increase in frequency at a rate of 20 dB/decade. This makes the circuit unstable. Also, the input impedance X_{C1} decreases with increase in frequency, which makes the circuit very susceptible to high-frequency noise. When amplified, this noise can completely override the differentiated output signal. The frequency response of the basic differentiator is shown in Figure . In this figure, f_a is the frequency at which the gain is 0 dB and is given by

$$f_a = \frac{1}{2\pi R_F C_1}$$



(a)

Also, f_c is the unity gain–bandwidth of the op-amp, and f is some relative operating frequency.

Both the stability and the high-frequency noise problems can be corrected by the addition of two components: R_1 and C_F, as shown in Figure . This circuit is a *practical differentiator*, the frequency response of which is shown in Figure 7-27(b) by a dashed line. From frequency f to f_b, the gain increases at 20 dB/decade. However, after f_b the gain decreases at 20 dB/decade. This 40-dB/decade change in gain is caused by the R_1C_1 and R_FC_F combinations. The gain-limiting frequency f_b is given by

$$f_b = \frac{1}{2\pi R_1 C_1} \qquad \text{where } R_1C_1 = R_FC_F.$$

turn R_1C_1 and R_FC_F values should be selected such that

$$f_a < f_b < f_c$$

$$f_a = \frac{1}{2\pi R_F C_1}$$

$$f_b = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_F C_F}$$

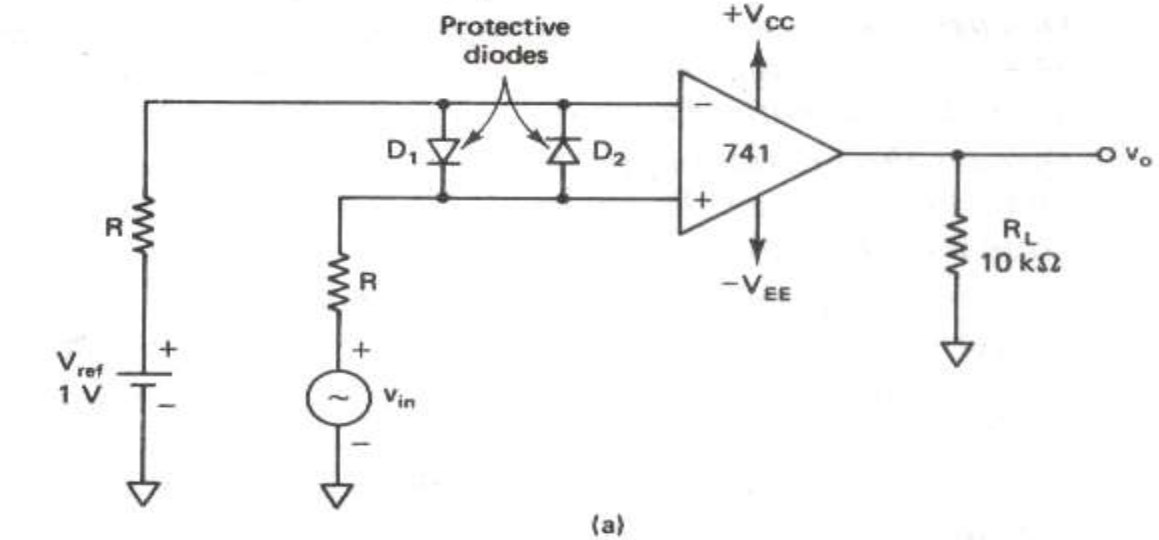
f_c = **unity gain–bandwidth**

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_F C_1$. That is,

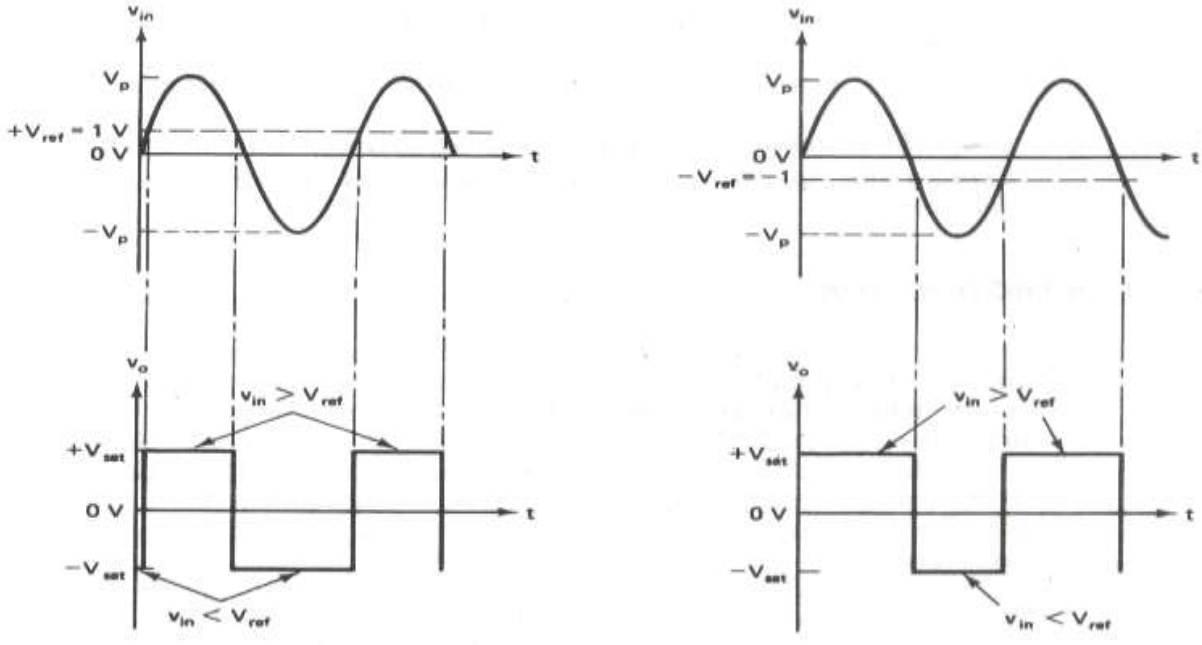
$$T \geq R_F C_1$$

BASIC COMPARATOR

Figure shows an op-amp used as a comparator. A fixed reference voltage V_{ref} of 1 V is applied to the (−) input, and the other time-varying signal voltage v_{in} is applied to the (+) input. Because of this arrangement, the circuit is called the *noninverting comparator.*



(a)



When v_{in} is less than V_{ref}, the output voltage v_o is at $-V_{sat}$ ($\cong -V_{EE}$) because the voltage at the (−) input is higher than that at the (+) input. On the other hand, when v_{in} is greater than V_{ref}, the (+) input becomes positive with respect to the (−) input, and v_o goes to $+V_{sat}$ ($\cong +V_{CC}$). Thus v_o changes from one saturation level to another whenever $v_{in} \cong V_{ref}$, as shown in Figure

ZERO-CROSSING DETECTOR

An immediate application of the comparator is the *zero-crossing detector* or *sine wave-to-square wave converter*.

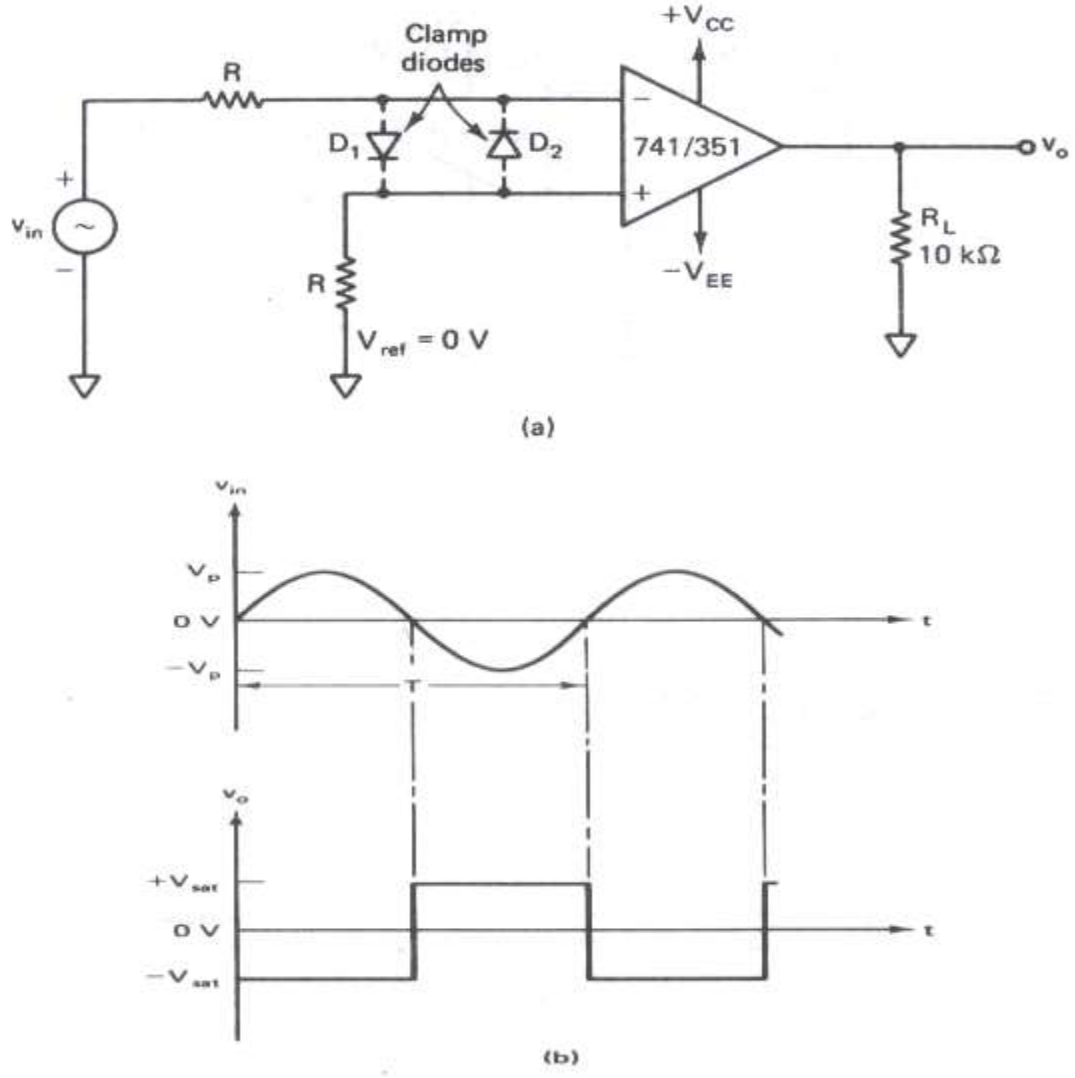


Figure 9–3 (a) Zero-crossing detector. (b) Its typical input and output waveforms.

SCHMITT TRIGGER

Figure shows an inverting comparator with *positive feedback*. This circuit converts an irregular-shaped waveform to a square wave or pulse. The circuit is known as the *Schmitt trigger* or squaring circuit. The input voltage v_{in} triggers

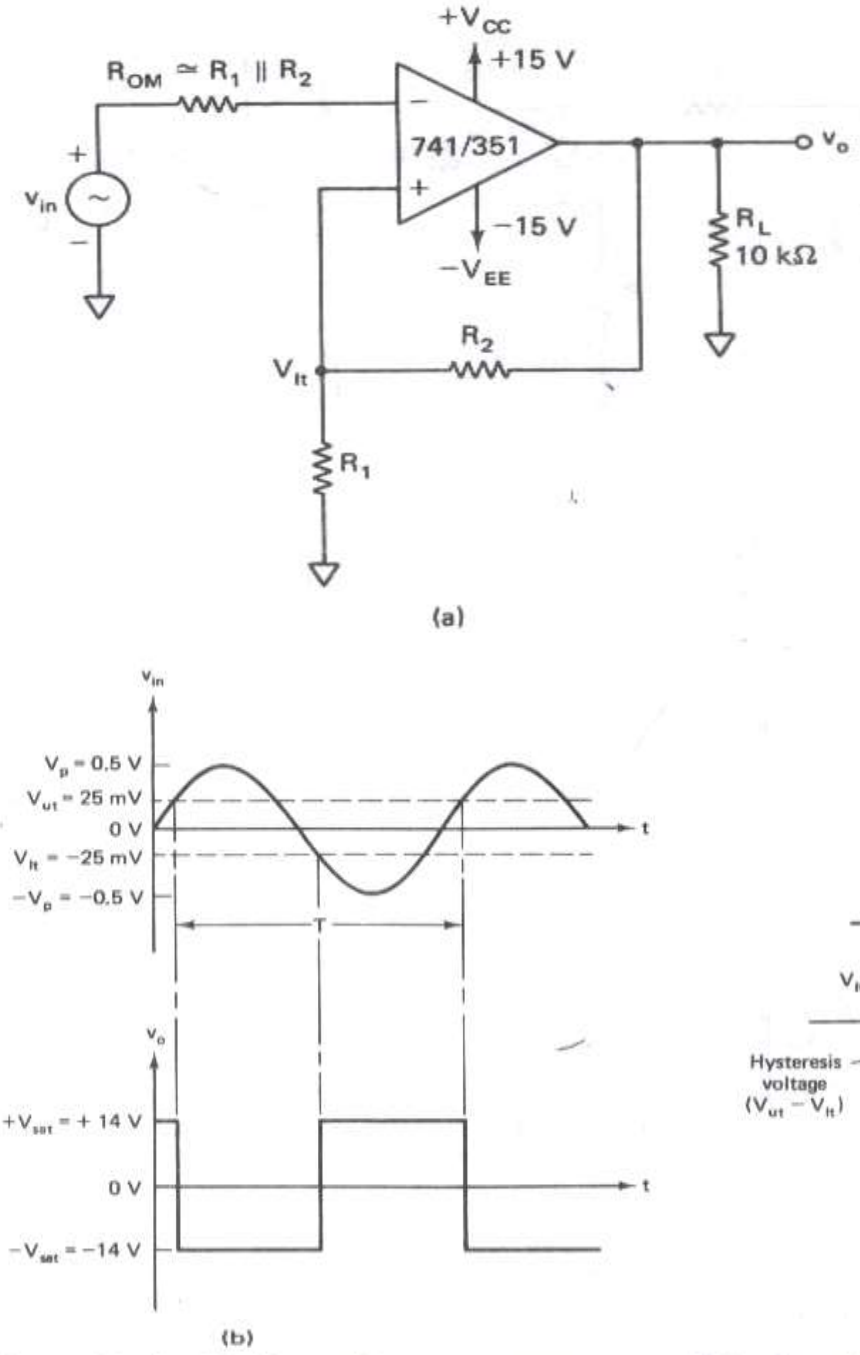


Figure 9–4 (a) Inverting comparator as Schmitt trigger. (b) Input and output waveforms of Schmitt trigger. (c) v_o versus v_{in} plot of the hysterisis voltage.

In Figure , these threshold voltages are obtained by using the voltage divider R_1–R_2, where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is a variable reference threshold voltage that depends on the value and polarity of the output voltage v_o. When $v_o = +V_{sat}$, the voltage across R_1 is called the *upper threshold voltage*, V_{ut}. The input voltage v_{in} must be slightly more positive than V_{ut} in order to cause the output v_o to switch from $+V_{sat}$ to $-V_{sat}$. As long as $v_{in} < V_{ut}$, v_o is at $+V_{sat}$. Using the voltage-divider rule,

$$V_{ut} = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

On the other hand, when $v_o = -V_{sat}$, the voltage across R_1 is referred to as *lower threshold voltage*, V_{lt}. v_{in} must be slightly more negative than V_{lt} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$. In other words, for v_{in} values greater than V_{lt}, v_o is at $-V_{sat}$. V_{lt} is given by the following equation:

$$V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

Thus, if the threshold voltages V_{ut} and V_{lt} are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions. Also, the positive feedback, because of its regenerative action, will make v_o switch faster between $+V_{sat}$ and $-V_{sat}$. In Figure , resistance $R_{OM} \cong R_1 \| R_2$ is used to minimize the offset problems.

The comparator with positive feedback is said to exhibit *hysteresis*, a dead-band condition. That is, when the input of the comparator exceeds V_{ut}, its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts back to its original state, $+V_{sat}$, when the input goes below V_{lt} . The hysteresis voltage is, of course, equal to the difference between V_{ut} and V_{lt}. Therefore,

$$V_{hy} = V_{ut} - V_{lt}$$

$$= \frac{R_1}{R_1 + R_2}[+V_{sat} - (-V_{at})]$$

SAMPLE-AND-HOLD CIRCUIT

The sample-and-hold circuit, as its name implies, samples an input signal and holds on to its last sampled value until the input is sampled again. Figure shows a sample-and-hold circuit using an op-amp with an E-MOSFET. In this circuit the E-MOSFET works as a switch that is controlled by the sample-and-hold control voltage V_S, and the capacitor C serves as a storage element. The circuit operates as follows. The analog signal v_{in} to be sampled is applied to the

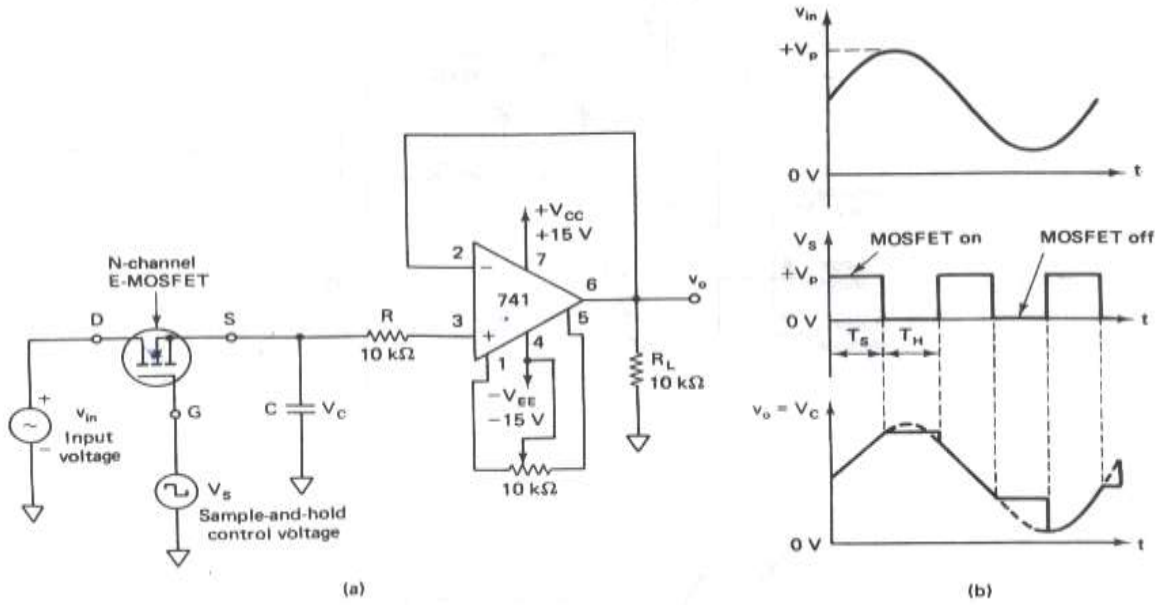


Figure 9–32 (a) Sample-and-hold circuit. (b) Its input and output waveforms.

drain, and sample-and-hold control voltage V_S is applied to the gate of the E-MOSFET. During the positive portion of V_S, the E-MOSFET conducts and acts as a closed switch. This allows input voltage to charge capacitor C. In other words, input voltage appears across C and in turn at the output, as shown in Figure On the other hand, when V_S is zero, the E-MOSFET is *off* (nonconductive) and acts as an open switch. The only discharge path for C is, therefore, through the op-amp. However, the input resistance of the op-amp voltage follower is also very high; hence the voltage across C is retained. The time periods T_S of the sample-and-hold control voltage V_S during which the voltage across the capacitor is equal to the input voltage are called *sample periods*. The time periods T_H of V_S during which the voltage across the capacitor is constant are called *hold periods* The output of the op-amp is usually processed/observed during hold periods. To obtain close approximation of the input waveform, the frequency of the sample-and-hold control voltage must be significantly higher than that of the input. In critical applications a precision and/or high-speed op-amp is helpful. If possible, choose a low-leakage capacitor such as Teflon or polyethylene.

SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Fig. Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig. fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage V_{ref} is βv_o and may take values as

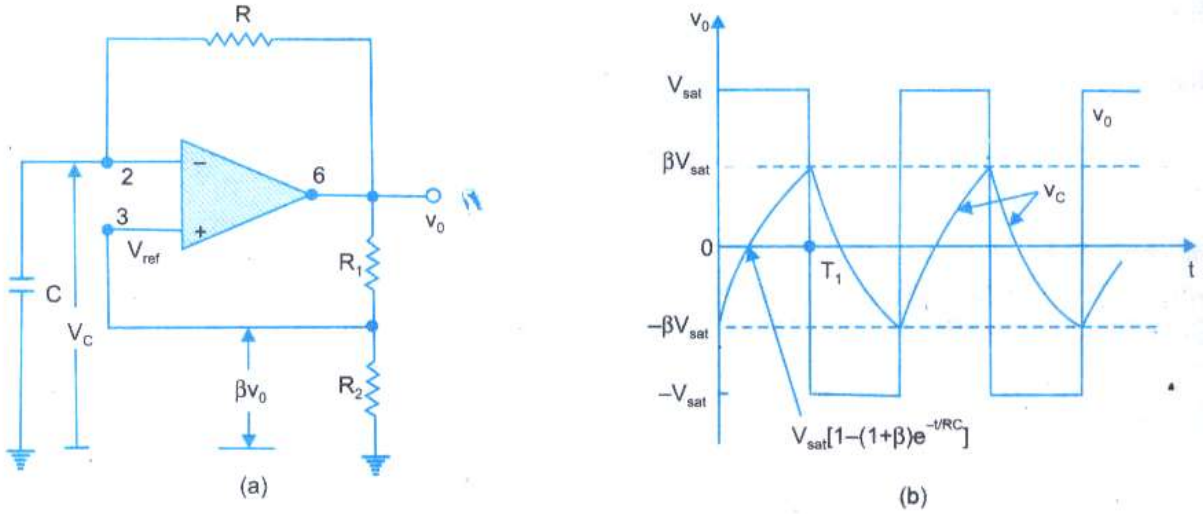


Fig. 5.10 (a) Simple op-amp square wave generator (b) waveforms

$+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fed back to the (–) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (–) input terminal just exceeds V_{ref}, switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at $+V_{sat}$. The capacitor now starts charging towards $+V_{sat}$ through resistance R, as shown in Fig. The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage. When the voltage at the (–) input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant, the voltage on the capacitor is $+\beta V_{sat}$. It begins to discharge through R, that is, charges toward $-V_{sat}$. When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats itself as shown in Fig. 5.10 (b).

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat}\,(1 + \beta)\, e^{-t/RC}$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place, Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC}$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1+\beta}{1-\beta}$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta}$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, it can be seen that $T = 2\ RC$

or

$$f_0 = \frac{1}{2RC}$$

The output swings from $+V_{sat}$ to $-V_{sat}$, so,

v_0 peak-to-peak $= 2\ V_{sat}$

MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. is a modified form of the astable multivibrator.

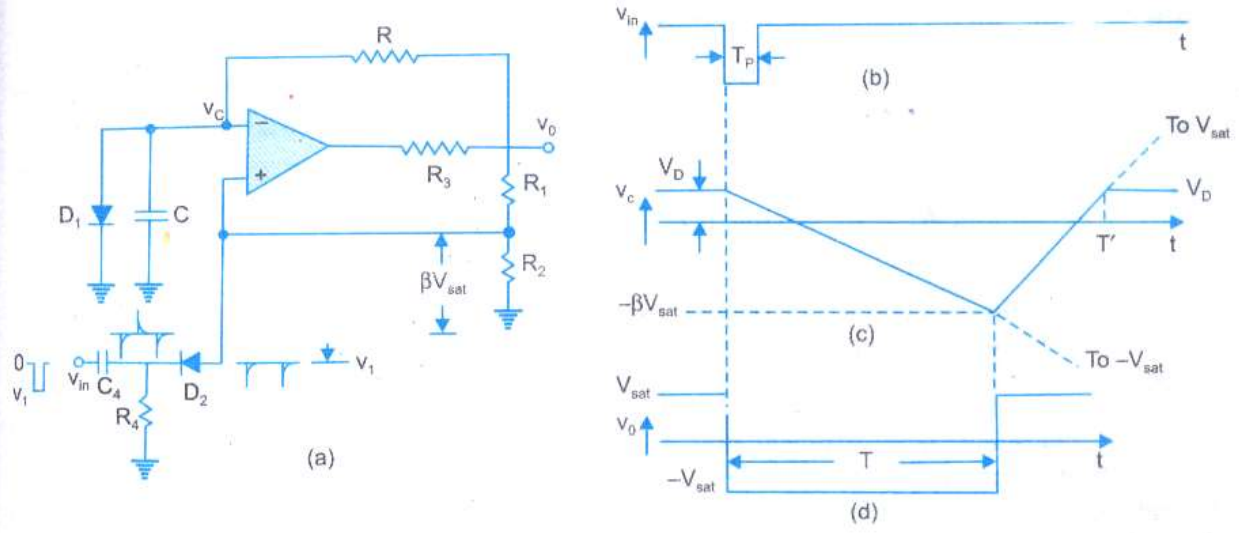


Fig. (a) Monostable multivibrator (b) negative going triggering signal (c) capacitor waveform (d) output voltage waveform

A diode D_1 clamps the capacitor voltage to 0.7V when the output is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

To analyse the circuit, let us assume that in the stable state, the output v_o is at $+V_{sat}$. The diode D_1 conducts and v_c the voltage across the capacitor C gets clamped to + 0.7V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+\beta V_{sat}$. Now, if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7V i.e. $([\beta V_{sat} + (-V_1)] < 0.7\ V)$, the output of the op-amp will switch from $+V_{sat}$ to $-V_{sat}$. The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$. When the capacitor voltage v_c becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until v_c is 0.7V as capacitor C gets clamped to the voltage. Various waveforms are shown in Fig. (b, c, d).

The pulse width T of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass RC circuit with V_i and V_f as initial and final values is,

$$v_o = V_f + (V_i - V_f)e^{-t/RC}$$

For the circuit, $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage).

The output v_c is,

$$v_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC}$$

at $t = T$,

$$v_c = -\beta V_{sat}$$

Therefore,

$$-\beta\, V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

After simplification, pulse width T is obtained as

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta}$$

where $\beta = R_2/(R_1 + R_2)$

If, $V_{sat} >> V_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$T = 0.69\ RC$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator. The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

Voltage Regulator

The function of a voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current. Voltage regulators are classified as:

Series regulator
Switching regulator

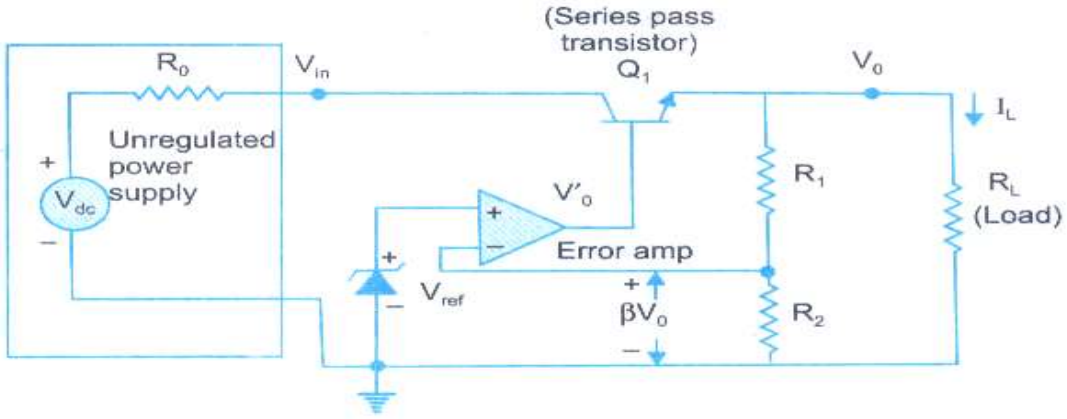
Series regulators use a power transistor connected in series between the unregulated dc input and the load. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor. Since the transistor conducts in the active or linear region, these regulators are also called linear regulators. Linear regulators may have fixed or variable output voltage and could be positive or negative. The schematic, important characteristics, data sheet, short circuit protection, current fold-back, current boosting techniques for linear voltage regulators such as 78 XX, 79 XX series, 723 IC are discussed.

Switching regulators, on the other hand, operate the power transistor as a high frequency ***on/off*** switch, so that the power transistor does not conduct current continuously.

SERIES OP-AMP REGULATOR

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations. Figure shows a regulated power supply using discrete components. The circuit consists of following four parts:

1. Reference voltage circuit
2. Error amplifier
3. Series pass transistor
4. Feedback network.



It can be seen from Fig. that the power transistor Q_1 is in series with the unregulated dc voltage V_{in} and the regulated output voltage V_o. So it must absorb the difference between these two voltages whenever any fluctuation in output voltage V_o occurs. The transistor Q_1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load. The output voltage is sampled by the $R_1 - R_2$ divider and fed back to the (–) input terminal of the op-amp error amplifier. This sampled voltage is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The output V_o' of the error amplifier drives the series transistor Q_1.

If the output voltage increases, say, due to variation in load current, the sampled voltage βV_0 also increases where

$$\beta = \frac{R_2}{R_1 + R_2}$$

This, in turn, reduces the output voltage V_0' of the diff-amp due to the 180° phase difference provided by the op-amp amplifier. V_0' is applied to the base of Q_1, which is used as an emitter follower. So V_0 follows V_0', that is V_0 also reduces. Hence the increase in V_0 is nullified. Similarly, reduction in output voltage also gets regulated.

IC VOLTAGE REGULATORS

With the advent of micro-electronics, it is possible to incorporate the complete circuit of Fig. on a monolithic silicon chip. This gives low cost, high reliability, reduction in size and excellent performance. Examples of monolithic regulators are 78 XX/79 XX series and 723 general purpose regulators.

78 XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V. In 78 XX, the last two numbers (XX) indicate the output voltage. Thus 7815 represents a 15 V regulator. There are also available 79 XX series of fixed output, negative voltage regulators which are complements to the 78 XX series devices. There are two extra voltage options of – 2 V and – 5.2 V available in 79 XX series. These regulators are available in two types of packages.

Metal package (TO – 3 type)
Plastic package (TO – 220 type)

723 GENERAL PURPOSE REGULATOR

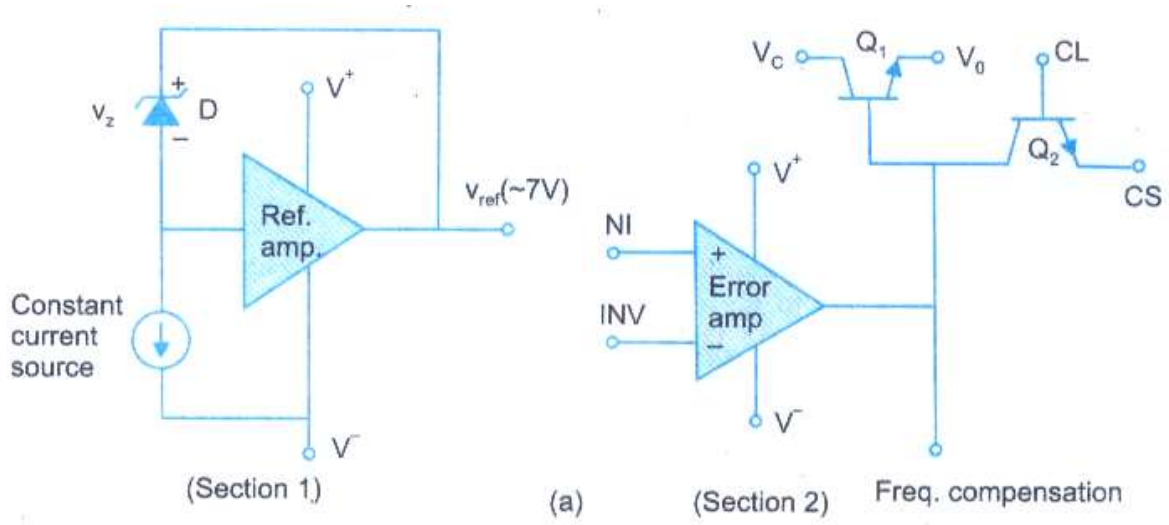
The three terminal regulators discussed earlier have the following limitations:

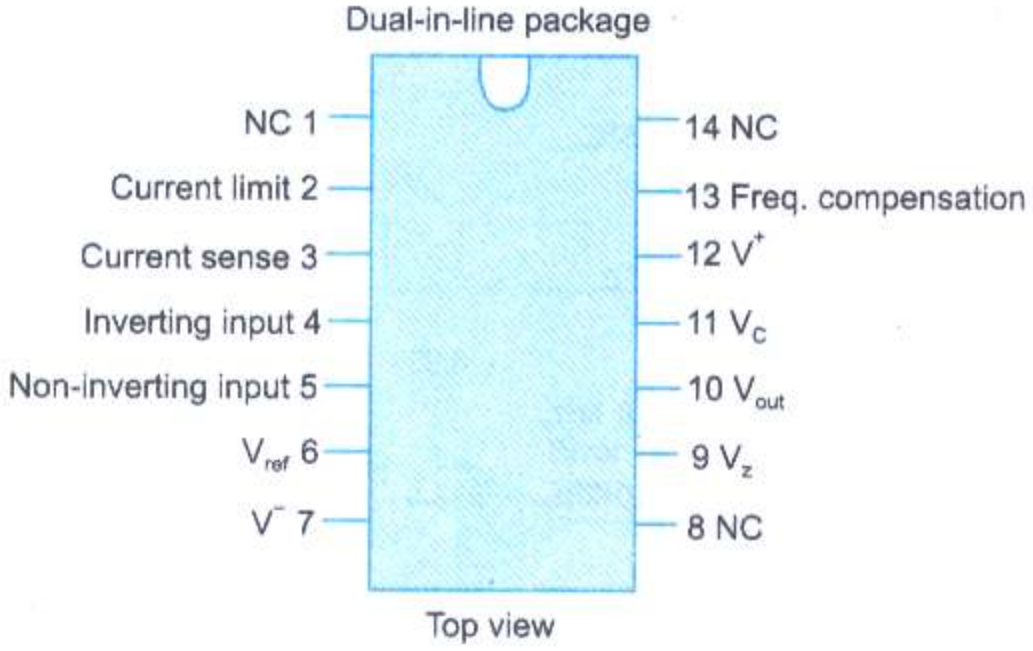
1. No short circuit protection
2. Output voltage (positive or negative) is fixed.

These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits.

Figure shows the functional block diagram of a 723 regulator IC. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref}. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage V_{ref} applied at the NI input terminal. The error signal controls the conduction of Q_1. These two sections are not internally connected but the various points are brought out on the IC package. 723 regulated IC is available in a 14-pin dual-in-line package or 10-pin metal-can as shown in Fig. important features and electrical characteristics are given in Table 6.2.





723 Voltage Regulator
Important Features:
*Input voltage 40V max
*Output voltage adjustable from 2V to 37V
*150 mA output current without external pass transistor
*Output currents in excess of 10A possible by adding external transistors
*Can be used as either a linear or a switching regulator